BiMOS

FCT INTERFACE LOGIC

HARRIS

Product Availability

For Information on Specific Device Types, Contact Your Nearest Harris Sales Office.

BIMOS FCT Interface Logic

Harris Semiconductor has developed a new family of products for TTL backplane-interface applications. Using a small-geometry BiMOS technology, these FCT bus-interface integrated circuits vastly reduce power consumption, avoid bus contention, minimize switching noise, and provide outputs that are specifically tailored to interface with VME buses or their equivalents.

This Data Book contains detailed technical information on the new FCT bus-interface integrated circuits. The first section, **Product Selectors,** provides a complete index to devices, product selection guide, cross-reference guide, packages, and ordering information.

A **Technical Overview** section describes the FCT family features, benefits, ratings and characteristics, and output capabilities.

A **Technical Data** section provides definitive ratings and characteristics data for individual types in the FCT bus-interface family. The data sheets are arranged in alphanumeric sequence.

The Data Book also contains an **Application Note** and **Dimensional Outlines** of the packages in which these products are supplied.

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Product Selectors

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CD54FCT241E/M	CD74FCT241E/M	CD54FCT241H	3-3	Octal Buffer/Line Driver, 3-State	20
CD54FCT244E/M	CD74FCT244E/M	CD54FCT244H	3-3	Octal Buffer/Line Driver, 3-State	20
CD54FCT245E/M	CD74FCT245E/M	CD54FCT245H	3-8	Octal Bus Transceiver, 3-State	20
CD54FCT273E/M	CD74FCT273E/M	CD54FCT273H	3-13	Octal D Flip-Flop with Reset	20
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CD54FCT533E/M	CD74FCT533E/M	CD54FCT533H	3-17	Octal Transparent Latch, 3-State, Inverting	20
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CD54FCT640E/M	CD74FCT640E/M	CD54FCT640H	3-56	Octal Bus Transceiver, 3-State, Inverting	20
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CD54FCT649EN/M	CD74FCT649EN/M	CD54FCT649H	3-66	Octal Bus Transceiver/Register, With Open Drain, Inverting	24
CD54FCT651EN/M	CD74FCT651EN/M	CD54FCT651H	3-71	Octal Bus Transceiver/Register, 3-State, Inverting	24
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CD54FCT653EN/M	CD74FCT653EN/M	CD54FCT653H	3-76	Octal Bus Transceiver/Register, Open-Drain (A Side), 3-State (B Side), Inverting	24
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CD54FCT821AEN/M	CD74FCT821AEN/M	CD54FCT821AH	3-82	10-Bit D-Type Flip-Flop, 3-State	24
CD54FCT822AEN/M	CD74FCT822AEN/M	CD54FCT822AH	3-82	10-Bit D-Type Flip-Flop, 3-State, Inverting	24
CD54FCT823AEN/M	CD74FCT823AEN/M	CD54FCT823AH	3-87	9-Bit D-Type Flip-Flop, 3-State	24
CD54FCT824AEN/M	CD74FCT824AEN/M	CD54FCT824AH	3-87	9-Bit D-Type Flip-Flop, 3-State, Inverting	24
CD54FCT827AEN/M	CD74FCT827AEN/M	CD54FCT827AH	3-92	10-Bit Buffer/Line Driver, 3-State	24
CD54FCT828AEN/M	CD74FCT828AEN/M	CD54FCT828AH	3-92	10-Bit Buffer/Line Driver, 3-State Inverting	24
CD54FCT841AEN/M	CD74FCT841AEN/M	CD54FCT841AH	3-97	10-Bit Transparent Latch, 3-State	24
CD54FCT842AEN/M	CD74FCT842AEN/M	CD54FCT842AH	3-97	10-Bit Transparent Latch, 3-State, Inverting	24
CD54FCT843AEN/M	CD74FCT843AEN/M	CD54FCT843AH	3-102	9-Bit Transparent Latch, 3-State	24

†Package Suffix
E - Dual-In-Line Plastic
EN - Dual-In-Line Narrow-Body Plastic
M - Small-Outline Plastic
H - Chip

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CD54FCT29520AEN/M	CD74FCT29520AEN/M	CD54FCT29520AH	3-127	Multilevel Pipeline Register	24
CD54FCT29521AEN/M	CD74FCT29521AEN/M	CD54FCT29521AH	3-127	Multilevel Pipeline Register	24

†Package Suffix
E - Dual-In-Line Plastic
EN - Dual-In-Line Narrow-Body Plastic
M - Small-Outline Plastic
H - Chip

Product Selection Guide

Cross-Reference Guide

Industry Type	Equivalent Bipolar Type	Harris Recommended Replacement
IDT74FCT240P	74F240P	CD74FCT240E
IDT74FCT241P	74F241P	CD74FCT241E
IDT74FCT244P	74F244P	CD74FCT244E
IDT74FCT245P	74F245P	CD74FCT245E
IDT74FCT273P	74F273P	CD74FCT273E
IDT74FCT373P	74F373P	CD74FCT373E
IDT74FCT374P	74F374P	CD74FCT374E
IDT74FCT377P	74F377P	CD74FCT377E
IDT74FCT533P	74F533P	CD74FCT533E
IDT74FCT534P	74F534P	CD74FCT534E
IDT74FCT540P	74F540P	CD74FCT540E
IDT74FCT541P	74F541P	CD74FCT541E
IDT74FCT543P	74F543SP	CD74FCT543EN
—	74F544SP	CD74FCT544EN
—	74F563P	CD74FCT563E
—	74F564P	CD74FCT564E
IDT74FCT573P	74F573P	CD74FCT573E
IDT74FCT574P	74F574P	CD74FCT574E
—	74F623P	CD74FCT623E
IDT74FCT640P	—	CD74FCT640E
—	—	CD74FCT643E
IDT74FCT646P	74F646SP	CD74FCT646EN
—	—	CD74FCT647EN
IDT74FCT648P	74F648SP	CD74FCT648EN
—	—	CD74FCT649EN
IDT74FCT651P	74F651SP	CD74FCT651EN
IDT74FCT652P	74F652SP	CD74FCT652EN
—	—	CD74FCT653EN
—	—	CD74FCT654EN
IDT74FCT821AP	74F821SP	CD74FCT821AEN
IDT74FCT822AP	—	CD74FCT822AEN
IDT74FCT823AP	74F823SP	CD74FCT823AEN
IDT74FCT824AP	—	CD74FCT824AEN
IDT74FCT827AP	74F827SP	CD74FCT827AEN
IDT74FCT828AP	74F828SP	CD74FCT828AEN
IDT74FCT841AP	74F841SP	CD74FCT841AEN
IDT74FCT842AP	—	CD74FCT842AEN
IDT74FCT843AP	74F843SP	CD74FCT843AEN
IDT74FCT844AP	—	CD74FCT844AEN
IDT74FCT861AP	—	CD74FCT861AEN
IDT74FCT862AP	—	CD74FCT862AEN
IDT74FCT863AP	—	CD74FCT863AEN
IDT74FCT864AP	—	CD74FCT864AEN
IDT29FCT52AP	—	CD74FCT2952AEN
IDT29FCT53AP	—	CD74FCT2953AEN
—	—	CD74FCT7623EN
IDT29FCT520AP	—	CD74FCT29520AEN
IDT29FCT521AP	—	CD74FCT29521AEN

Industry Type	Equivalent Bipolar Type	Harris Recommended Replacement
IDT54FCT240P	54F240P	CD54FCT240E
IDT54FCT241P	54F241P	CD54FCT241E
IDT54FCT244P	54F244P	CD54FCT244E
IDT54FCT245P	54F245P	CD54FCT245E
IDT54FCT273P	54F273P	CD54FCT273E
IDT54FCT373P	54F373P	CD54FCT373E
IDT54FCT374P	54F374P	CD54FCT374E
IDT54FCT377P	54F377P	CD54FCT377E
IDT54FCT533P	54F533P	CD54FCT533E
IDT54FCT534P	54F534P	CD54FCT534E
IDT54FCT540P	54F540P	CD54FCT540E
IDT54FCT541P	54F541P	CD54FCT541E
IDT54FCT543P	54F543SP	CD54FCT543EN
—	54F544SP	CD54FCT544EN
—	54F563P	CD54FCT563E
—	54F564P	CD54FCT564E
IDT54FCT573P	54F573P	CD54FCT573E
IDT54FCT574P	54F574P	CD54FCT574E
—	54F623P	CD54FCT623E
IDT54FCT640P	—	CD54FCT640E
—	—	CD54FCT643E
IDT54FCT646P	54F646SP	CD54FCT646EN
—	—	CD54FCT647EN
IDT54FCT648P	54F648SP	CD54FCT648EN
—	—	CD54FCT649EN
IDT54FCT651P	54F651SP	CD54FCT651EN
IDT54FCT652P	54F652SP	CD54FCT652EN
—	—	CD54FCT653EN
—	—	CD54FCT654EN
IDT54FCT821AP	54F821SP	CD54FCT821AEN
IDT54FCT822AP	—	CD54FCT822AEN
IDT54FCT823AP	54F823SP	CD54FCT823AEN
IDT54FCT824AP	—	CD54FCT824AEN
IDT54FCT827AP	54F827SP	CD54FCT827AEN
IDT54FCT828AP	54F828SP	CD54FCT828AEN
IDT54FCT841AP	54F841SP	CD54FCT841AEN
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IDT54FCT843AP	54F843SP	CD54FCT843AEN
IDT54FCT844AP	—	CD54FCT844AEN
IDT54FCT861AP	—	CD54FCT861AEN
IDT54FCT862AP	—	CD54FCT862AEN
IDT54FCT863AP	—	CD54FCT863AEN
IDT54FCT864AP	—	CD54FCT864AEN
IDT29FCT52ABP	—	CD54FCT2952AEN
IDT29FCT53ABP	—	CD54FCT2953AEN
—	—	CD54FCT7623EN
IDT29FCT520ABP	—	CD54FCT29520AEN
IDT29FCT521ABP	—	CD54FCT29521AEN

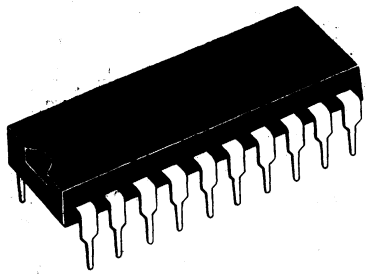
Cross-Reference Guide (Cont'd)

Industry Type	Equivalent Bipolar Type	Harris Recommended Replacement
IDT74FCT240SO	74F240S	CD74FCT240M
IDT74FCT241SO	74F241S	CD74FCT241M
IDT74FCT244SO	74F244S	CD74FCT244M
IDT74FCT245SO	74F245S	CD74FCT245M
IDT74FCT273SO	74F273S	CD74FCT273M
IDT74FCT373SO	74F373S	CD74FCT373M
IDT74FCT374SO	74F374S	CD74FCT374M
IDT74FCT377SO	74F377S	CD74FCT377M
IDT74FCT533SO	74F533S	CD74FCT533M
IDT74FCT534SO	74F534S	CD74FCT534M
IDT74FCT540SO	74F540S	CD74FCT540M
IDT74FCT541SO	74F541S	CD74FCT541M
IDT74FCT543SO	74F543S	CD74FCT543M
—	74F544S	CD74FCT544M
—	74F563S	CD74FCT563M
—	74F564S	CD74FCT564M
IDT74FCT573SO	74F573S	CD74FCT573M
IDT74FCT574SO	74F574S	CD74FCT574M
—	74F623S	CD74FCT623M
IDT74FCT640SO	—	CD74FCT640M
—	—	CD74FCT643M
IDT74FCT646SO	74F646S	CD74FCT646M
—	—	CD74FCT647M
IDT74FCT648SO	74F648S	CD74FCT648M
—	—	CD74FCT649M
IDT74FCT651SO	74F651S	CD74FCT651M
IDT74FCT652SO	74F652S	CD74FCT652M
—	—	CD74FCT653M
—	—	CD74FCT654M
IDT74FCT821ASO	74F821S	CD74FCT821AM
IDT74FCT822ASO	—	CD74FCT822AM
IDT74FCT823ASO	74F823S	CD74FCT823AM
IDT74FCT824ASO	—	CD74FCT824AM
IDT74FCT827ASO	74F827S	CD74FCT827AM
IDT74FCT828ASO	74F828S	CD74FCT828AM
IDT74FCT841ASO	74F841S	CD74FCT841AM
IDT74FCT842ASO	—	CD74FCT842AM
IDT74FCT843ASO	74F843S	CD74FCT843AM
IDT74FCT844ASO	—	CD74FCT844AM
IDT74FCT861ASO	—	CD74FCT861AM
IDT74FCT862ASO	—	CD74FCT862AM
IDT74FCT863ASO	—	CD74FCT863AM
IDT74FCT864ASO	—	CD74FCT864AM
IDT29FCT52ASO	—	CD74FCT2952AM
IDT29FCT53ASO	—	CD74FCT2953AM
—	—	CD74FCT7623M
IDT29FCT520ASO	—	CD74FCT29520AM
IDT29FCT521ASO	—	CD74FCT29531AM

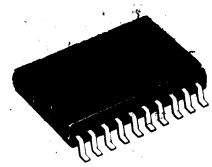
Industry Type	Equivalent Bipolar Type	Harris Recommended Replacement
IDT54FCT240SO	54F240S	CD54FCT240M
IDT54FCT241SO	54F241S	CD54FCT241M
IDT54FCT244SO	54F244S	CD54FCT244M
IDT54FCT245SO	54F245S	CD54FCT245M
IDT54FCT273SO	54F273S	CD54FCT273M
IDT54FCT373SO	54F373S	CD54FCT373M
IDT54FCT374SO	54F374S	CD54FCT374M
IDT54FCT377SO	54F377S	CD54FCT377M
IDT54FCT533SO	54F533S	CD54FCT533M
IDT54FCT534SO	54F534S	CD54FCT534M
IDT54FCT540SO	54F540S	CD54FCT540M
IDT54FCT541SO	54F541S	CD54FCT541M
IDT54FCT543SO	54F543S	CD54FCT543M
—	54F544S	CD54FCT544M
—	54F563S	CD54FCT563M
—	54F564S	CD54FCT564M
IDT54FCT573SO	54F573S	CD54FCT573M
IDT54FCT574SO	54F574S	CD54FCT574M
—	54F623S	CD54FCT623M
IDT54FCT640SO	—	CD54FCT640M
—	—	CD54FCT643M
IDT54FCT646SO	54F646S	CD54FCT646M
—	—	CD54FCT647M
IDT54FCT648SO	54F648S	CD54FCT648M
—	—	CD54FCT649M
IDT54FCT651SO	54F651S	CD54FCT651M
IDT54FCT652SO	54F652S	CD54FCT652M
—	—	CD54FCT653M
—	—	CD54FCT654M
IDT54FCT821ASO	54F821S	CD54FCT821AM
IDT54FCT822ASO	—	CD54FCT822AM
IDT54FCT823ASO	54F823S	CD54FCT823AM
IDT54FCT824ASO	—	CD54FCT824AM
IDT54FCT827ASO	54F827S	CD54FCT827AM
IDT54FCT828ASO	54F828S	CD54FCT828AM
IDT54FCT841ASO	54F841S	CD54FCT841AM
IDT54FCT842ASO	—	CD54FCT842AM
IDT54FCT843ASO	54F843S	CD54FCT843AM
IDT54FCT844ASO	—	CD54FCT844AM
IDT54FCT861ASO	—	CD54FCT861AM
IDT54FCT862ASO	—	CD54FCT862AM
IDT54FCT863ASO	—	CD54FCT863AM
IDT54FCT864ASO	—	CD54FCT864AM
IDT29FCT52ABSO	—	CD54FCT2952AM
IDT29FCT53ABSO	—	CD54FCT2953AM
—	—	CD54FCT7623M
IDT29FCT520ABSO	—	CD54FCT29520AM
IDT29FCT521ABSO	—	CD54FCT29521AM

Packages

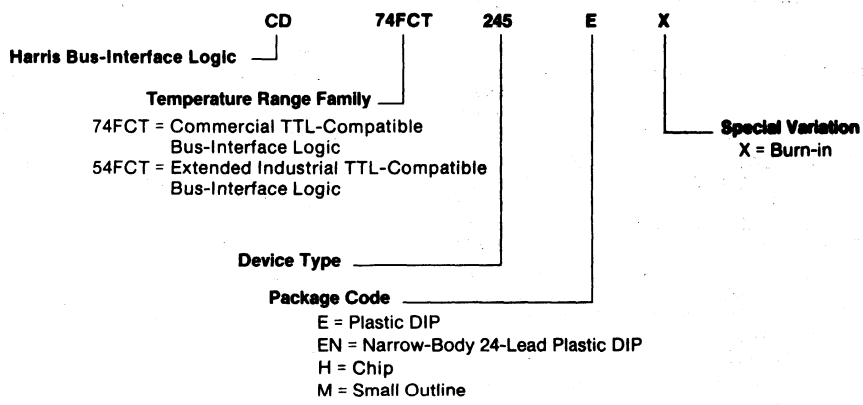
Typical Dual-In-Line Plastic Package



Typical SO (Small Outline) Plastic Package



Ordering Information



Temperature Range
All packages when properly derated can be operated from -55 to +125°C.
At low temperature, limit for E, EN, and M packages is -55°C.

Package Outlines
Dimensions for the packages shown above are given in the Dimensional Outlines section.

Technical Overview 2

Technical Overview

FCT PRODUCTS FOR BACKPLANE-INTERFACE APPLICATIONS

Harris FCT products are developed to provide a reliable interface with modern high-speed backplanes. The FCT types vastly reduce power consumption, avoid bus contention, minimize switching noise, and provide outputs that are specifically tailored to interface with VME buses or their equivalents.

The speed of the FCT family is comparable to that of bipolar FAST types, Sink current ranges from 48 milliamperes to 64 milliamperes depending on product type. Fully populated buses, such as the 21-slot VME can be reliably interfaced. Products are most economically packaged in plastic DIP and gull-wing surface-mount pinouts. As with the Harris AC/ACT family of logic devices, simultaneous switching transients are controlled to levels comparable to similar bipolar logic functions (1 volt peak area for octal ground bounce.).

FCT products, the modern standard for backplane-interface applications, meet or exceed published JEDEC industry-standard No. 18 specifications. FCT products clearly are the low-power backplane interface needed in the rapidly growing down-sized computer world, where low operating power and virtually zero standby power are essential requirements.

The two competitive bipolar families (FAST and BCT), compared with FCT products, are 150 times higher in quiescent power consumption and 10 times higher in operating power consumption at a continuous five megahertz operation. This comparison is illustrated on page 2-3.

Two other salient features of this FCT design are: 1) The ratio of sink-to-source current minimizes bus contention; and 2) The absence of clamp diodes to the positive supply rail prevents high-current drain during power-down, thereby permitting PCB insertion when the power is on.

Table I lists types and type numbers.

FCT Features

Speed	Competitive with similar bipolar F/AS TTL functions. Typical delay is 3.5 nanoseconds.
Sink/Source Current	All types have sink and source currents meeting VME, multibus, etc standards. Output edges are monotonic through the TTL switch point with fully populated backplanes. A BiMOS output driver stage is used.
Simultaneous Switching Transient	(Ground bounce) Competitive with similar bipolar TTL and CMOS products Output swing is 3.5 volts. Controlled output-edge rate.
Operating and Standby Power	Ultra-low pure CMOS operating power and standby power of almost zero.
Pinout	Standard

FCT Benefits

Swift delay requirements dictated by modern control-system backplane-interface logic present no problems.

Optimized output drives minimize backplane reflections in worst-case situations.

EMI and RFI emissions minimized. Good signal-pulse integrity.

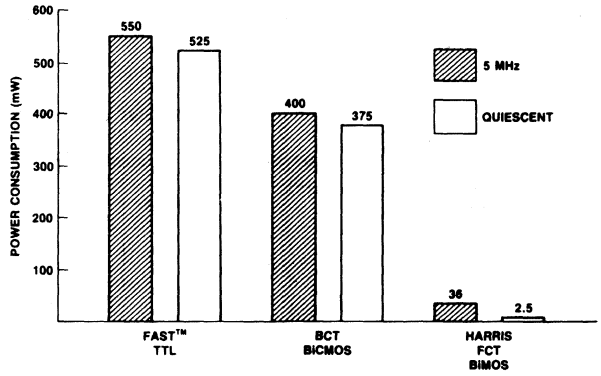
Meets low-power needs of down-sized computers without fans, etc. Low battery drain.

Provided in minimum and most economically sized DIP and SOP.

Minimum CAD/CAM, burn-in board, and PC-board real-estate costs with no performance sacrifice.

Table I - FCT Types

Buffers			
CD54/74FCT240	CD54/74FCT241	CD54/74FCT244	CD54/74FCT540
CD54/74FCT541	CD54/74FCT827A	CD54/74FCT828A	
Transceivers			
CD54/74FCT245	CD54/74FCT543	CD54/74FCT544	CD54/74FCT623
CD54/74FCT640	CD54/74FCT643	CD54/74FCT646	CD54/74FCT647
CD54/74FCT648	CD54/74FCT649	CD54/74FCT651	CD54/74FCT652
CD54/74FCT653	CD54/74FCT654	CD54/74FCT861A	CD54/74FCT862A
CD54/74FCT863A	CD54/74FCT864A	CD54/74FCT2952A	CD54/74FCT2953A
CD54/74FCT7623			
Latches			
CD54/74FCT373	CD54/74FCT533	CD54/74FCT563	CD54/74FCT573
CD54/74FCT841A	CD54/74FCT842A	CD54/74FCT843A	CD54/74FCT844A
Registers			
CD54/74FCT377	CD54/74FCT821A	CD54/74FCT822A	CD54/74FCT823A
CD54/74FCT824A	CD54/74FCT29520A	CD54/74FCT29521A	
Flip-Flops			
CD54/74FCT273	CD54/74FCT374	CD54/74FCT534	CD54/74FCT564
CD54/74FCT574			



Comparison of power consumption for an octal transceiver type.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (V_{CC}) ..... **-0.5 to 6 V**
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ V) ..... **-20 mA**
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ V) ..... **-50 mA**
DC OUTPUT SINK CURRENT per Output Pin, I_O ..... **+70 mA**
DC OUTPUT SOURCE CURRENT per Output Pin, I_O ..... **-30 mA**
DC V_{CC} CURRENT (I_{CC}) ..... **N (I_{OH}) + M (ΔI_{CC}) mA**
DC GROUND CURRENT (I_{GND}) ..... **N (I_{OL}) + M (ΔI_{CC}) mA**
where N = No. of outputs
M = No. of inputs

POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C (PACKAGE TYPE E) ..... **500 mW**
For T_A = +100 to +125°C (PACKAGE TYPE E) ..... **Derate Linearly at 8 mW/°C to 300 mW**
For T_A = -55 to +70°C (PACKAGE TYPE M) ..... **400 mW**
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... **Derate Linearly at 6 mW/°C to 70 mW**
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE E, M ..... **-55 to +125°C**
STORAGE TEMPERATURE (T_{stg}) ..... **-65 to +150°C**
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... **+265°C**
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only ..... **+300°C**

RECOMMENDED OPERATING CONDITIONS:
The following are normal operating ranges for these devices. For maximum reliability, devices should always be operated within these ranges.

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V_{CC}*:			
T_A = 0 to 70°C	4.75	5.25	V
T_A = -55 to + 125°C	4.5	5.5	
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A	-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv	0	10	ns/V

*Unless otherwise specified, all voltages are referenced to ground.

STATIC ELECTRICAL CHARACTERISTICS
FCT Series:

74FCT Commercial Temperature Range, 0 to 70°C. V_{CC} max = 5.25 V, V_{CC} min = 4.75 V

54FCT Extended Industrial Temperature Range, -55 to +125°C. V_{CC} max = 5.5 V, V_{CC} min = 4.5 V

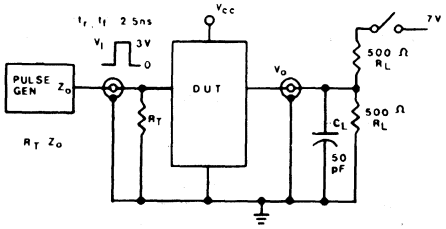
CHARACTERISTICS		TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
					+25		0 to +70		-55 to +125		
		V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage	V_{IL}			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage	V_{OH}	V_{IH} or V_{IL}	-15#	MIN.	2.4	—	2.4	—	—	—	V
			-12#		2.4	—	—	—	2.4	—	
Low-Level Output Voltage	V_{OL}	V_{IH} or V_{IL}	64#	MIN.	—	0.55	—	0.55	—	—	
			48#		—	0.55	—	—	—	0.55	
High-Level Input Current	I_{IH}	V_{CC}		MAX.	—	0.1	—	1	—	1	μA
Low-Level Input Current	I_{IL}	GND		MAX.	—	-0.1	—	-1	—	-1	μA
3-State Leakage Current	I_{OZH}	V_{CC}		MAX.	—	0.5	—	10	—	10	μA
	I_{OZL}	GND		MAX.	—	-0.5	—	-10	—	-10	
Short-Circuit Output Current*	I_{OS}	V_{CC} or GND V_O = 0		MAX.	-60#	—	-60#	—	-60#	—	mA
Input Clamp Voltage	V_{IK}	V_{CC} or GND	-18	MIN.	—	-1.2	—	-1.2	—	-1.2	V
Quiescent Supply Current, MSI	I_{CC}	V_{CC} or GND	0	MAX.	—	8	—	80	—	500	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load	ΔI_{CC}	3.4 V†		MAX.	—	1.6	—	1.6	—	2	mA

*Not more than one output should be shorted at one time. Test duration should not exceed 100 ms.
†Inputs that are not measured are at V_{CC} or Gnd.

FCT Input Loading: All inputs are 1 unit load. Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 1.6 mA max. @ 70°C.
#Values are for FCT240 types (see "Output Capabilities" and Table II for I_{OS}, I_{OL}, and I_{OH} for other types.)

SWITCHING WAVEFORMS FOR 54/74FCTXXX

Shown below is the FCT test circuit. A Thevenin equivalent may be used for output loading.

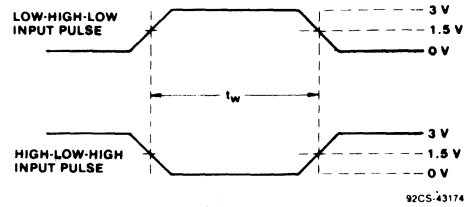


TEST	SWITCH POSITION
t_{PLZ} t_{PZL} OPEN DRAIN	CLOSED
t_{PHZ} t_{PZH} t_{PLH} t_{PHL}	OPEN

Definitions:

C_L = Load capacitance includes jig and probe capacitance.
R_T = Termination should be equal to Z_{OUT} of the pulse generator. (Typically 50 Ω).
V_{IN} = 0 V to 3 V
Input: t_r = t_f = 2.5 ns (10% to 90%) unless otherwise specified.

Test circuit.



Output Requirement:

Device must follow truth table.
$V_{OL} \leq 0.55$ V
$V_{OH} \geq 2.4$ V

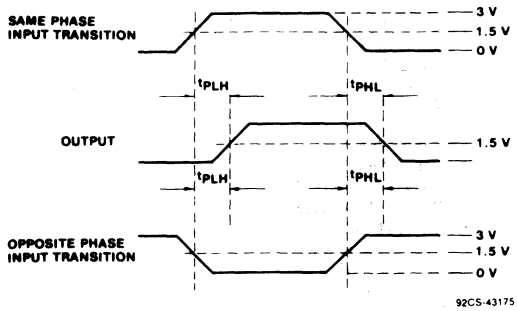
Input Condition:

$t_r = t_f \leq 2.5$ ns (as fast as required)

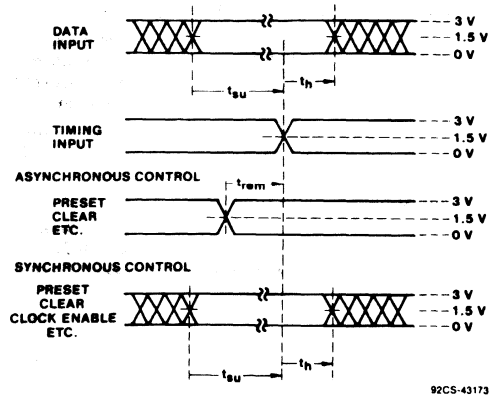
Standard Output Loading:

R_L = 500 Ω
C_L = 50 pF

Input pulse width.



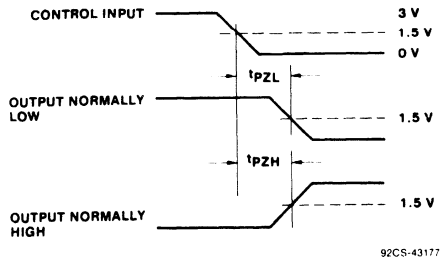
Propagation delay times.



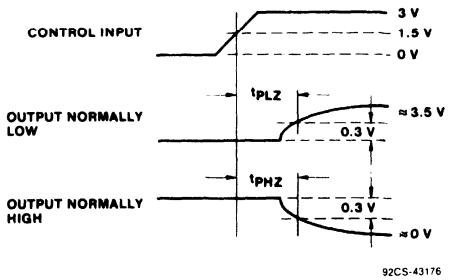
Setup, hold, and removal times.

SWITCHING WAVEFORMS FOR 54/74FCTXXX (CONT'D)

ENABLE TIMES



DISABLE TIMES



Output enable and disable times.

OUTPUT CAPABILITIES

Because of the numerous applications for 54/74FCT types, the output specifications are derived from the LOW drive and HIGH drive tables below. Any I_{OL} type category may be combined with any I_{OH} and I_{OS} type category to specify the output drive. Refer to Table II for device type categories.

Minimum Output at Low Drive (I_{OL}); V_{CC} = min

Type Category	Low-Level Output Voltage V_{OL} (V)	Minimum Low-Level Output Current I_{OL} (mA)	
		COM'L	MIL
3	0.55	48	32
4	0.55	64	48

Minimum Output at High Drive (I_{OH}); V_{CC} = min

Type Category	High-Level Output Voltage V_{OH} (V)	Minimum High-Level Output Current I_{OH} (mA)	
		COM'L	MIL
1	2.4	-15	-12
2	2.4	-24	-20

Minimum Output at Short Circuit (I_{OS}); V_{CC} = max

Type Category	Output Voltage V_O (V)	Minimum Short-Circuit Output Current I_{OS} (mA)	
		COM'L	MIL
1	0.0	-60	-60
2	0.0	-75	-75

Table II - Output Drive for 54/74FCTXXX

Device Number	I_{OH} Output Type	I_{OL} Output Type
54/74FCT240	1	4
54/74FCT241	1	4
54/74FCT244	1	4
54/74FCT245	1	4
54/74FCT273	1	3
54/74FCT373	1	3
54/74FCT374	1	3
54/74FCT377	1	3
54/74FCT533	1	3
54/74FCT534	1	3
54/74FCT540	1	4
54/74FCT541	1	4
54/74FCT563	1	3
54/74FCT564	1	3
54/74FCT573	1	3
54/74FCT574	1	3
54/74FCT623/7623	1	4
54/74FCT646	1	4
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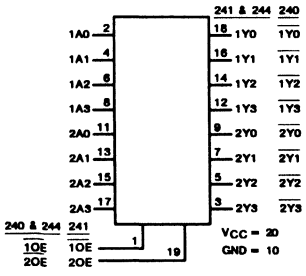
54/74FCT653	1	4
54/74FCT654	1	4
54/74FCT821A-824A	2	3
54/74FCT827A-828A	2	3
54/74FCT841A-844A	2	3
54/74FCT861A-864A	2	3
54/74FCT2952A	1	4
54/74FCT2953A	1	4
54/74FCT29520A	2	3
54/74FCT29521A	2	3

Technical Data

3

CD54/74FCT240, CD54/74FCT241 CD54/74FCT244



FUNCTIONAL DIAGRAM

Octal Buffers/Line Drivers, 3-State

CD54/74FCT240 - Inverting
CD54/74FCT241 - Non-Inverting
CD54/74FCT244 - Non-Inverting

Type Features:

- *Buffered inputs*
- *Typical propagation delay: 3ns @ V_{CC} = 5V, T_A = +25°C, C_L = 50pF*

3

The CD54/74FCT240, CD54/74FCT241, and CD54/74FCT244 3-state octal buffers/line drivers use a small-geometry BiMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output-HIGH level to two diode drops below V_{CC}. This resultant lowering of output swing (0V to 3.7V) reduces power bus ringing (a source of EMI) and minimizes V_{CC} bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 48 to 64 milliamperes.

The CD54/74FCT240 and CD54/74FCT244 have active-LOW output enables ($\overline{1OE}$, $\overline{2OE}$). The CD54/74FCT241 has one active-LOW ($\overline{1OE}$) and one active-HIGH (2OE) output enable.

The CD54/74FCT240, CD54/74FCT241, and CD54/74FCT244 are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over two temperature ranges: Commercial (0°C to +70°C) and Extended Industrial (-55°C to +125°C).

Family Features:

- *SCR-latchup-resistant CMOS process and circuit design*
- *Speed of bipolar FAST*/AS/S with significantly reduced power consumption*
- *64/48-mA output sink current (commercial/extended industrial)*
- *Output voltage swing limited to 3.7V @ V_{CC} = 5V*
- *Controlled output-edge rates*
- *Input/output isolation to V_{CC}*
- *BiMOS technology with low quiescent power*

* FAST is a registered trademark of Fairchild Semiconductor Corp.

The CD54FCT240, CD54FCT241, and CD54FCT244 are also available in chip form (H suffix). These unpackaged devices are operable over the -55°C to +125°C temperature range.

TRUTH TABLES

INPUTS		OUTPUT
$\overline{1OE}$, $\overline{2OE}$	A	$\overline{Y}$
L	L	H
L	H	L
H	X	Z

(FCT240)

INPUTS		OUTPUT	INPUTS		OUTPUT
$\overline{1OE}$	1A	1Y	2OE	2A	2Y
L	L	L	L	X	Z
L	H	H	H	L	L
H	X	Z	H	H	H

(FCT241)

INPUTS		OUTPUT
$\overline{1OE}$, $\overline{2OE}$	A	Y
L	L	L
L	H	H
H	X	Z

(FCT244)

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = HIGH Impedance

Printed in USA/8-89

File Number **2227**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (V_{CC}) ..... -0.5V to 6V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5V$) ..... -20mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5V$) ..... -50mA
DC OUTPUT SINK CURRENT per Output Pin, I_O ..... +70mA
DC OUTPUT SOURCE CURRENT per Output Pin, I_O ..... -30mA
DC V_{CC} CURRENT (I_{CC}) 140mA
DC GROUND CURRENT (I_{GND}) 528mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55°C to +100°C (PACKAGE TYPE E) 500mW
For T_A = +100°C to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8mW/°C to 300mW
For T_A = -55°C to +70°C (PACKAGE TYPE M) 400mW
For T_A = +70°C to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6mW/°C to 70mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE E, M ..... -55°C to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 in. ± 1/32 in. (1.59mm ± 0.79mm) from case for 10s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59mm) with solder contacting lead tips only ..... +300°C

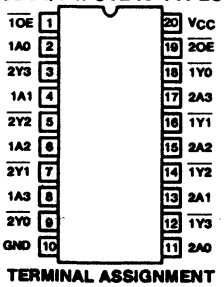
RECOMMENDED OPERATING CONDITIONS:

The following are normal operating ranges for these devices. For maximum reliability, devices should always be operated within these ranges.

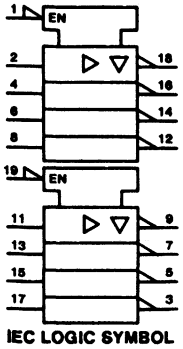
CHARACTERISTIC		LIMITS MIN	LIMITS MAX	UNITS
Supply-Voltage Range, V_{CC}*:	CD74 Series, T_A = 0°C to 70°C	4.75	5.25	V
	CD54 Series, T_A = -55°C to +125°C	4.5	5.5	V
DC Input Voltage, V_I		0	V_{CC}	V
DC Output Voltage, V_O		0	$\leq V_{CC}$	V
Operating Temperature, T_A		-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv		0	10	ns/V

* Unless otherwise specified, all voltages are referenced to ground.

CD54/74FCT240 TYPES

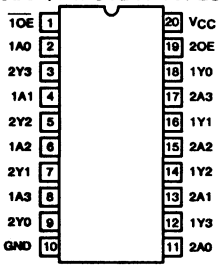


TERMINAL ASSIGNMENT



IEC LOGIC SYMBOL

CD54/74FCT241 TYPES



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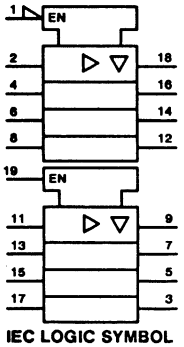
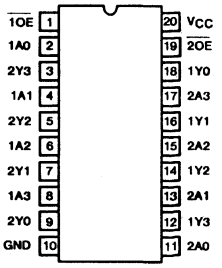
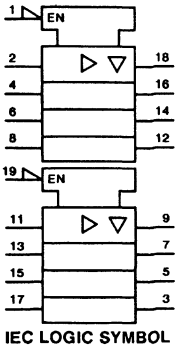


IEC LOGIC SYMBOL

CD54/74FCT244 TYPES



TERMINAL ASSIGNMENT



IEC LOGIC SYMBOL

STATIC ELECTRICAL CHARACTERISTICS

FCT Series: 74FCT Commercial Temperature Range, 0°C to +70°C; V_{CC} max = 5.25V, V_{CC} min = 4.75V
54FCT Extended Industrial Temperature Range, -55°C to +125°C; V_{CC} max = 5.5V, V_{CC} min = 4.5V

CHARACTERISTICS		TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A)						UNITS
					+25°C		0°C to +70°C		-55°C to +125°C		
		V_I (V)	I_O (mA)		MIN	MAX	MIN	MAX	MIN	MAX	
High-Level Input Voltage	V_{IH}			4.5 to 5.5	2	-	2	-	2	-	V
Low-Level Input Voltage	V_{IL}			4.5 to 5.5	-	0.8	-	0.8	-	0.8	V
High-Level Output Voltage	V_{OH}	V_{IH} or	-15	MIN	2.4	-	2.4	-	-	-	V
		V_{IL}	-12	MIN	2.4	-	-	-	2.4	-	V
Low-Level Output Voltage	V_{OL}	V_{IH} or	64	MIN	-	0.55	-	0.55	-	-	V
		V_{IL}	48	MIN	-	0.55	-	-	-	0.55	V
High-Level Input Current	I_{IH}	V_{CC}		MAX	-	0.1	-	1	-	1	µA
Low-Level Input Current	I_{IL}	GND		MAX	-	-0.1	-	-1	-	-1	µA
3-State Leakage Current	I_{OZH}	V_{CC}		MAX	-	0.5	-	10	-	10	µA
	I_{OZL}	GND		MAX	-	-0.5	-	-10	-	-10	µA
Short-Circuit Output Current *	I_{OS}	V_{CC} or GND V_O = 0		MAX	-60	-	-60	-	-60	-	mA
Input Clamp Voltage	V_{IK}	V_{CC} or GND	-18	MIN	-	-1.2	-	-1.2	-	-1.2	V
Quiescent Supply Current, MSI	I_{CC}	V_{CC} or GND	0	MAX	-	8	-	80	-	500	µA
Additional Quiescent Supply Current per Input Pin TTL Inputs High, 1 Unit Load	ΔI_{CC}	3.4V†		MAX	-	1.6	-	1.6	-	2	mA

* Not more than one output should be shorted at one time. Test duration should not exceed 100ms.
† Inputs that are not measured are at V_{CC} or GND.

FCT Input Loading: All inputs are 1 unit load. Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 1.6mA max. @ +70°C.

SWITCHING CHARACTERISTICS

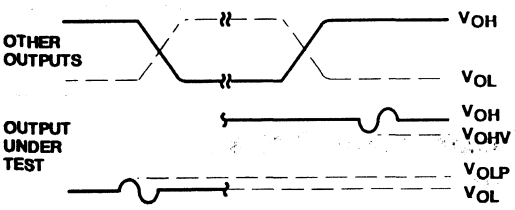
FCT Series: t_r, t_f = 2.5ns, C_L = 50pF, R_L - See Figure 2

CHARACTERISTICS		SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) 0°C to +70°C MIN	0°C to +70°C MAX	-55°C to +125°C MIN	-55°C to +125°C MAX	UNITS
Propagation Delays: Data to Outputs	FCT240	t_{PLH}, t_{PHL}	5†	1.5	8	1.5	9	ns
	FCT241, FCT244	t_{PLH}, t_{PHL}	5	1.5	6.5	1.5	7	ns
Output Enable Times	FCT240	t_{PZL}, t_{PZH}	-	1.5	10	1.5	10.5	ns
	FCT241, FCT244	t_{PZL}, t_{PZH}	-	1.5	8	1.5	8.5	ns
Output Disable Times	FCT240	t_{PLZ}, t_{PHZ}	-	1.5	9.5	1.5	12.5	ns
	FCT241, FCT244	t_{PLZ}, t_{PHZ}	-	1.5	7	1.5	7.5	ns
Power Dissipation Capacitance	FCT240, FCT241	C_{PD}§	-	65 Typical				pF
	FCT244	C_{PD}§	-	65 Typical				pF
Min. (Valley) V_{OHV} During Switching of Other Outputs (Output Under Test Not Switching)		V_{OHV} See Figure 1	5	0.5 Typical @ +25°C				V
Max. (Peak) V_{OLP} During Switching of Other Outputs (Output Under Test Not Switching)		V_{OLP} See Figure 1	5	1 Typical @ +25°C				V
Input Capacitance		C_I	-	-	10	-	10	pF
3-State Output Capacitance		C_O	-	-	15	-	15	pF

†5V: min. is @ 5.5V
max. is @ 4.5V
5V: min. is @ 5.25V for 0°C to +70°C
max. is @ 4.75V for 0°C to +70°C

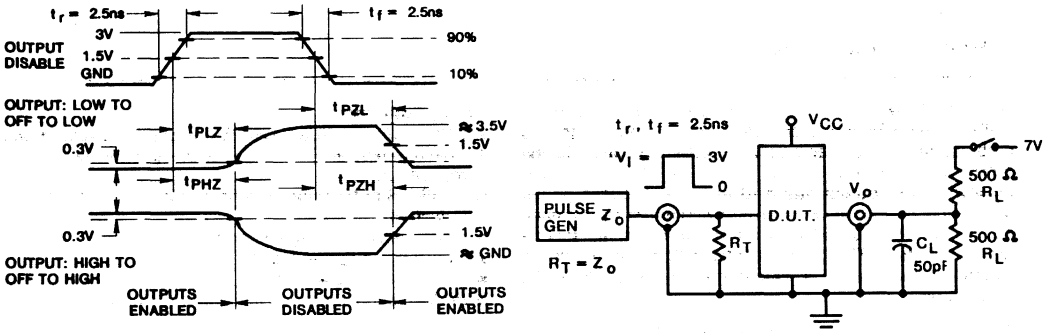
§C_{PD}, measured per function, is used to determine the dynamic power consumption.
P_D (per package) = V_{CC} I_{CC} + Σ (V_{CC}^2 f_i C_{PD} + V_O^2 f_o C_L + V_{CC} ΔI_{CC}D) where:
V_{CC} = supply voltage
ΔI_{CC} = flow through current x unit load
C_L = output load capacitance
D = duty cycle of input high
f_o = output frequency
f_i = input frequency

PARAMETER MEASUREMENT INFORMATION



NOTES:
1. V_{OLP} is measured with respect to a ground reference near the output under test. V_{OHV} is measured with respect to V_{OH}.
2. Input pulses have the following characteristics: PRR ≤ 1MHz, t_r = 2.5ns, t_f = 2.5ns, skew 1ns.
3. R.F. fixture with 700-MHz design rules required. IC should be soldered into test board and bypassed with 0.1μF capacitor. Scope and probes require 700-MHz bandwidth.

Figure 1 - Simultaneous switching transient waveforms.



TEST	SWITCH POSITION
t_{PLZ}, t_{PZL}, OPEN DRAIN	CLOSED
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	OPEN

Figure 2 - Three-state propagation delay times and test circuit.

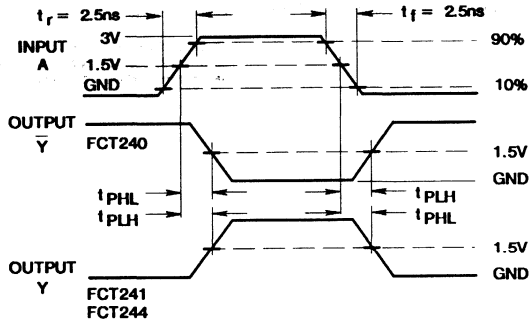
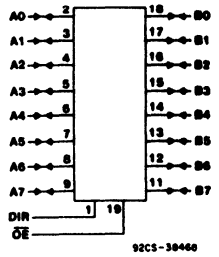


Figure 3 - Propagation delay times.

CD54/74FCT245



FUNCTIONAL DIAGRAM

Octal-Bus Transceiver, 3-State, Non-Inverting

Type Features:
- *Buffered inputs*
- *Typical propagation delay: 3 ns @ V_{CC} = 5 V, T_A = 25°C, C_L = 50 pF*

The CD54/74FCT245 octal-bus transceivers use a small-geometry BiMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output-HIGH level to two diode drops below V_{CC}. This resultant lowering of output swing (0 to 3.7 V) reduces power bus ringing (a source of EMI) and minimizes V_{CC} bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 48 to 64 milliamperes.

The CD54/74FCT245 are non-inverting, 3-state, bidirectional transceiver-buffers intended for two-way transmission from "A" bus to "B" bus or "B" bus to "A" bus. The logic level present on the Direction input (DIR) determines the data direction. When the Output Enable input ($\overline{OE}$) is HIGH, the outputs are in the high-impedance state.

The CD54/74FCT245 are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over two temperature ranges: Commercial (0 to 70°C) and Extended Industrial (-55 to +125°C).

The CD54FCT245 is also available in chip form (H suffix). This unpackaged device is operable over the -55 to +125°C temperature range.

Family Features:
- *SCR-latchup-resistant CMOS process and circuit design*
- *Speed of bipolar FAST*/AS/S with significantly reduced power*
- *64/48-mA output sink current (commercial/extended industrial)*
- *Output voltage swing limited to 3.7 V @ V_{CC} = 5 V*
- *Controlled output-edge rates*
- *Input/output isolation to V_{CC}*
- *BiMOS technology with low quiescent power*

*FAST is a Registered Trademark of Fairchild Semiconductor Corp.

TRUTH TABLE

CONTROL INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B DATA TO A BUS
L	H	A DATA TO B BUS
H	X	ISOLATION

H = high level, L = low level, X = irrelevant

To prevent excess currents in the High-Z (isolation) modes, all I/O terminals should be terminated with 10 kΩ to 1 MΩ resistors.

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File Number 2301

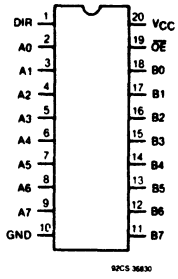
MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE (V_{CC}) ..... -0.5 to 6 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ V) ..... -20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ V) ..... -50 mA
DC OUTPUT SINK CURRENT per Output Pin, I_O ..... +70 mA
DC OUTPUT SOURCE CURRENT per Output Pin, I_O ..... -30 mA
DC V_{CC} CURRENT (I_{CC}) ..... 140 mA
DC GROUND CURRENT (I_{GND}) ..... 528 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE E, M ..... -55 to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only ..... +300°C

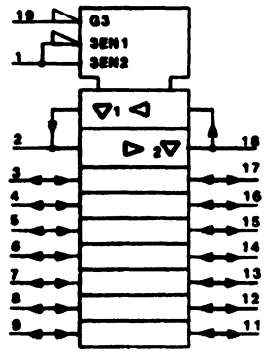
RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply Voltage Range, V_{CC}*:			
CD74 Series, T_A = 0 to 70°C	4.75	5.25	V
CD54 Series, T_A = -55 to +125°C	4.5	5.5	
DC Input Voltage, V_I	0	V_{CC}	
DC Output Voltage, V_O	0	$\leq V_{CC}$	
Operating Temperature, T_A	-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv	0	10	ns/V

*Unless otherwise specified, all voltages are referenced to ground.



TERMINAL ASSIGNMENT



IEC LOGIC SYMBOL

STATIC ELECTRICAL CHARACTERISTICS
FCT Series:

74FCT Commercial Temperature Range, 0 to 70°C; V_{CC} max = 5.25 V, V_{CC} min = 4.75 V

54FCT Extended Industrial Temperature Range, -55 to +125°C; V_{CC} max = 5.5 V, V_{CC} min = 4.5 V

CHARACTERISTICS		TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
					+25		0 to +70		-55 to +125		
		V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage	V_{IL}			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage	V_{OH}	V_{IH} or V_{IL}	-15	MIN.	2.4	—	2.4	—	—	—	V
			-12		2.4	—	—	—	2.4	—	
Low-Level Output Voltage	V_{OL}	V_{IH} or V_{IL}	64	MIN.	—	0.55	—	0.55	—	—	
			48		—	0.55	—	—	—	0.55	
High-Level Input Current	I_{IH}	V_{CC}		MAX.	—	0.1	—	1	—	1	μA
Low-Level Input Current	I_{IL}	GND		MAX.	—	-0.1	—	-1	—	-1	μA
3-State Leakage Current	I_{OZH}	V_{CC}		MAX.	—	0.5	—	10	—	10	μA
	I_{OZL}	GND		MAX.	—	-0.5	—	-10	—	-10	
Short-Circuit Output Current*	I_{OS}	V_{CC} or GND V_O = 0		MAX.	-60	—	-60	—	-60	—	mA
Input Clamp Voltage	V_{IK}	V_{CC} or GND	-18	MIN.	—	-1.2	—	-1.2	—	-1.2	V
Quiescent Supply Current, MSI	I_{CC}	V_{CC} or GND	0	MAX.	—	8	—	80	—	500	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load	ΔI_{CC}	3.4 V†		MAX.	—	1.6	—	1.6	—	2	mA

*Not more than one output should be shorted at one time. Test duration should not exceed 100 ms.
†Inputs that are not measured are at V_{CC} or Gnd.

FCT Input Loading: All inputs are 1 unit load. Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 1.6 mA max. @ 70°C.

SWITCHING CHARACTERISTICS: t_r, t_f = 2.5 ns, C_L = 50 pF, R_L - See Fig. 3

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) -°C				UNITS
			0 to +70		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Data to Outputs	t_{PLH} t_{PHL}	5†	1.5	7	1.5	7.5	ns
Output Disable to Output	t_{PLZ} t_{PHZ}	5	1.5	7.5	1.5	10	ns
Output Enable to Output	t_{PZH} t_{PZL}	5	1.5	9.5	1.5	10	ns
Power Dissipation Capacitance	C_{PD}§	—					pF
Min. (Valley) V_{OHV} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OHV} See Fig. 1	5	0.5 Typ. @ 25°C				V
Max. (Peak) V_{OLP} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OLP} See Fig. 1	5	1 Typ. @ 25°C				V
Input Capacitance	C_I	—	—	10	—	10	pF
3-State Output Capacitance	C_O	—	—	15	—	15	pF

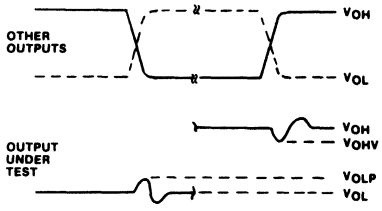
†5 V: min. is @ 5.5 V
max. is @ 4.5 V

5 V: min. is @ 5.25 V for 0 to +70°C
max. is @ 4.75 V for 0 to +70°C

§C_{PD}, measured per latch, is used to determine the dynamic power consumption.
P_D (per package) = V_{CC} I_{cc} + Σ (V_{CC}^2 f_i C_{PD} + V_o^2 f_o C_L + V_{CC} ΔI_{CC}D)
where V_{cc} = supply voltage
ΔI_{CC} = flow through current x unit load
C_L = output load capacitance
D = duty cycle of input high
f_o = output frequency
f_i = input frequency

3

PARAMETER MEASUREMENT INFORMATION



NOTES:
1. V_{OLP} IS MEASURED WITH RESPECT TO A GROUND REFERENCE NEAR THE OUTPUT UNDER TEST. V_{OHV} IS MEASURED WITH RESPECT TO V_{OH}.
2. INPUT PULSES HAVE THE FOLLOWING CHARACTERISTICS: PRR ≤ 1 MHz, t_r = 3 ns, t_f = 3 ns, SKEW 1 ns.
3. R.F. FIXTURE WITH 700-MHz DESIGN RULES REQUIRED. IC SHOULD BE SOLDERED INTO TEST BOARD AND BYPASSED WITH 0.1 μF CAPACITOR. SCOPE AND PROBES REQUIRE 700-MHz BANDWIDTH.

92CS-42406R1

Fig. 1 - Simultaneous switching transient waveforms.

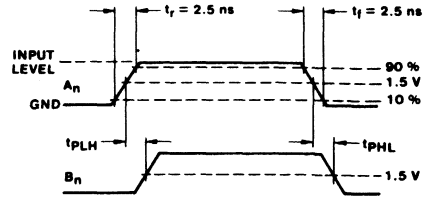
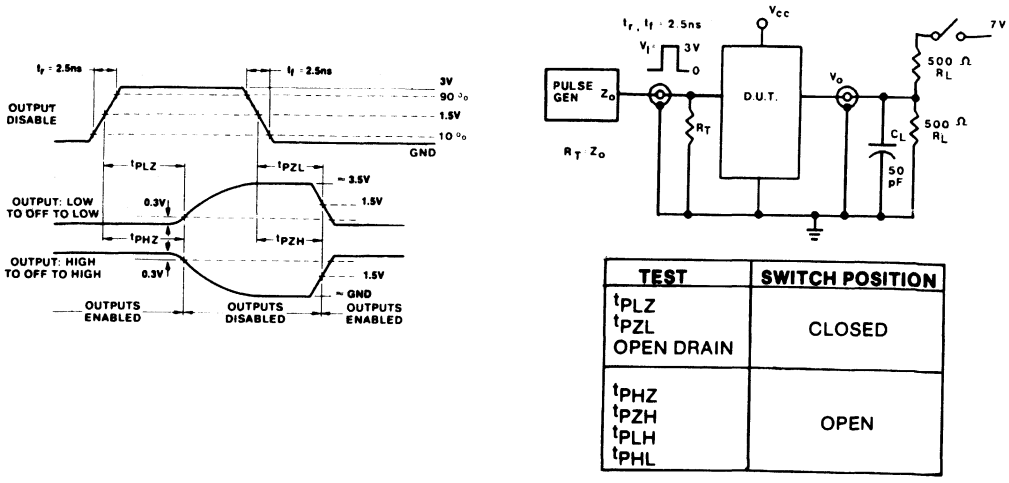


Fig. 2 - Propagation delay times.

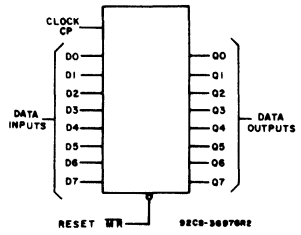


TEST	SWITCH POSITION
t_{PLZ} t_{PZL} OPEN DRAIN	CLOSED
t_{PHZ} t_{PZH} t_{PLH} t_{PHL}	OPEN

Fig. 3 - Three-state propagation delay times and test circuit.

CD54/74FCT273

Octal D Flip-Flop with Reset



FUNCTIONAL DIAGRAM

Type Features:
- *Buffered inputs*
- *Typical propagation delay: 4.5 ns @ V_{CC} = 5 V, T_A = 25°C, C_L = 50 pF*

3

The CD54/74FCT273 octal D flip-flops with reset use a small-geometry BiMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output-HIGH level to two diode drops below V_{CC}. This resultant lowering of output swing (0 to 3.7 V) reduces power bus ringing (a source of EMI) and minimizes V_{CC} bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 32 to 48 milliamperes.

Information at the D Input of the CD54/74FCT273 is transferred to the Q output on the positive-going edge of the clock pulse. All eight flip-flops are controlled by a common clock (CP) and common reset ($\overline{MR}$). Resetting is accomplished by a low voltage level independent of the clock.

The CD54/74FCT273 are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over two temperature ranges: Commercial (0 to 70°C) and Extended Industrial (-55 to +125°C).

The CD54FCT273 is also available in chip form (H suffix). This unpackaged device is operable over the -55 to +125°C temperature range.

Family Features:
- *SCR-latchup-resistant CMOS process and circuit design*
- *Speed of bipolar FAST*/AS/S with significantly reduced power consumption*
- *48/32-mA output sink current (commercial/extended industrial)*
- *Output voltage swing limited to 3.7 V @ V_{CC} = 5 V*
- *Controlled output-edge rates*
- *Input/output isolation to V_{CC}*
- *BiMOS technology with low quiescent power*

*FAST is a Registered Trademark of Fairchild Semiconductor Corp.

TRUTH TABLE (EACH FLIP-FLOP)

INPUTS			OUTPUTS
RESET ($\overline{MR}$)	CLOCK CP	DATA Dn	Qn
L	X	X	L
H	⎍	H	H
H	⎍	L	L
H	L	X	Qo

H = High level (steady state)
L = Low level (steady state)
X = Irrelevant
⎍ = Transition from low to high level
Qo = The level of Q before the indicated steady-state input conditions were established

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File Number **2303**

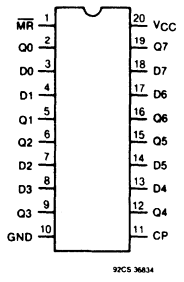
MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE (V_{CC}) ..... -0.5 to 6 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ V) ..... -20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ V) ..... -50 mA
DC OUTPUT SINK CURRENT per Output Pin, I_O ..... +70 mA
DC OUTPUT SOURCE CURRENT per Output Pin, I_O ..... -30 mA
DC V_{CC} CURRENT (I_{CC}) ..... 140 mA
DC GROUND CURRENT (I_{GND}) ..... 400 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE E, M ..... -55 to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only ..... +300°C

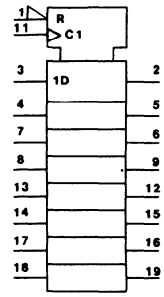
RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V_{CC}*:			
CD74 Series, T_A = 0 to 70°C	4.75	5.25	V
CD54 Series, T_A = -55 to +125°C	4.5	5.5	
DC Input Voltage, V_I	0	V_{CC}	
DC Output Voltage, V_O	0	$\leq V_{CC}$	
Operating Temperature, T_A	-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv	0	10	ns/V

*Unless otherwise specified, all voltages are referenced to ground.



TERMINAL ASSIGNMENT



IEC LOGIC SYMBOL

STATIC ELECTRICAL CHARACTERISTICS
FCT Series:

74FCT Commercial Temperature Range, 0 to 70°C; V_{CC} max = 5.25 V, V_{CC} min = 4.75 V
54FCT Extended Industrial Temperature Range, -55 to +125°C; V_{CC} max = 5.5 V, V_{CC} min = 4.5 V

CHARACTERISTICS		TEST CONDITIONS V_I (V)	TEST CONDITIONS I_O (mA)	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C: +25 MIN.	+25 MAX.	0 to +70 MIN.	0 to +70 MAX.	-55 to +125 MIN.	-55 to +125 MAX.	UNITS
High-Level Input Voltage	V_{IH}			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage	V_{IL}			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage	V_{OH}	V_{IH} or V_{IL}	-15	MIN.	2.4	—	2.4	—	—	—	V
			-12		2.4	—	—	—	2.4	—	
Low-Level Output Voltage	V_{OL}	V_{IH} or V_{IL}	48	MIN.	—	0.55	—	0.55	—	—	
			32		—	0.55	—	—	—	0.55	
High-Level Input Current	I_{IH}	V_{CC}		MAX.	—	0.1	—	1	—	1	μA
Low-Level Input Current	I_{IL}	GND		MAX.	—	-0.1	—	-1	—	-1	μA
3-State Leakage Current	I_{OZH}	V_{CC}		MAX.	—	0.5	—	10	—	10	μA
	I_{OZL}	GND		MAX.	—	-0.5	—	-10	—	-10	
Short-Circuit Output Current*	I_{OS}	V_{CC} or GND V_O = 0		MAX.	-60	—	-60	—	-60	—	mA
Input Clamp Voltage	V_{IK}	V_{CC} or GND	-18	MIN.	—	-1.2	—	-1.2	—	-1.2	V
Quiescent Supply Current, MSI	I_{CC}	V_{CC} or GND	0	MAX.	—	8	—	80	—	500	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load	ΔI_{CC}	3.4 V†		MAX.	—	1.6	—	1.6	—	2	mA

*Not more than one output should be shorted at one time. Test duration should not exceed 100 ms.
†Inputs that are not measured are at V_{CC} or Gnd.

FCT Input Loading: All inputs are 1 unit load. Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 1.6 mA max. @ 70°C.

3

PREREQUISITE FOR SWITCHING:

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) -°C				UNITS
			0 to +70		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Data to CP Setup Time	t_{SU}	5*	3	—	3.5	—	ns
Hold Time	t_H	5	2	—	2	—	ns
Removal Time $\overline{MR}$ to CP	t_{REM}	5	4	—	5	—	ns
$\overline{MR}$ Pulse Width	t_W	5	7	—	7	—	ns
CP Pulse Width	t_W	5	7	—	7	—	ns
CP Frequency	f_{max}	5	70	—	70	—	MHz

*min. is @ 4.5 V
min., is @ 4.75 V for 0 to +70°C

SWITCHING CHARACTERISTICS: t_r, t_f = 2.5 ns, C_L = 50 pF, R_L - See Fig. 4

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) -°C				UNITS
			0 to +70		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: CP to Qn	t_{PLH} t_{PHL}	5*	2	13	2	15	ns
$\overline{MR}$ to Qn	t_{PLH} t_{PLH}	5	2	13	2	15	ns
Power Dissipation Capacitance	C_{PD}†	—					pF
Input Capacitance	C_I	—	—	10	—	10	pF

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

5 V: min. is @ 5.25 V for 0 to +70°C
max. is @ 4.75 V for 0 to +70°C

§C_{PD}, measured per flip-flop, is used to determine the dynamic power consumption.
P_D (per package) = V_{CC} I_{cc} + Σ (V_{CC}^2 f_i C_{PD} + V_o^2 f_o C_L + V_{CC} ΔI_{CC}D)
where V_{cc} = supply voltage
ΔI_{CC} = flow-through current x unit load
C_L = output load capacitance
D = duty cycle of input high
f_o = output frequency
f_i = input frequency

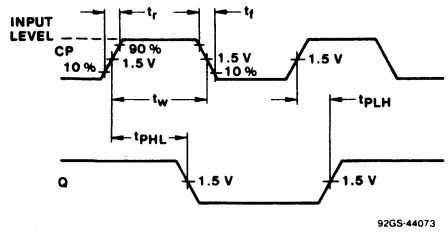


Fig. 1 - Propagation delay times and clock pulse width.

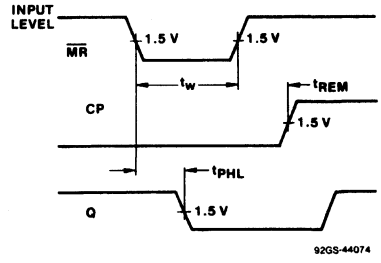


Fig. 2 - Prerequisite and propagation delay times for master reset.

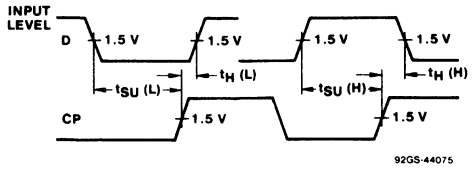


Fig. 3 - Prerequisite for clock.

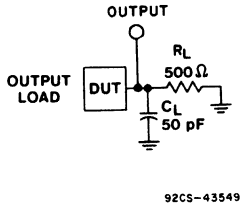
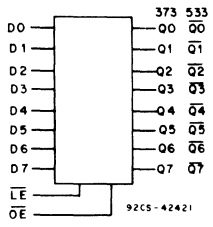


Fig. 4 - Test circuit.

CD54/74FCT373, CD54/74FCT533



FUNCTIONAL DIAGRAM

Octal Transparent Latch, 3-State

CD54/74FCT373 - Non-Inverting
CD54/74FCT533 - Inverting

Type Features:

- *Buffered inputs*
- *Typical propagation delay: 3.5 ns @ V_{CC} = 5 V, T_A = 25°C, C_L = 50 pF*

3

The CD54/74FCT373 and CD54/74FCT533 octal transparent latches use a small-geometry BiMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output-HIGH level to two diode drops below V_{CC}. This resultant lowering of output swing (0 to 3.7V) reduces power bus ringing (a source of EMI) and minimizes V_{CC} bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 32 to 48 milliamperes.

The CD54/74FCT373 and CD54/74FCT533 outputs are transparent to the inputs when the Latch Enable ($\overline{LE}$) is HIGH. When the Latch Enable ($\overline{LE}$) goes LOW, the data is latched. The Output Enable ($\overline{OE}$) controls the 3-state outputs. When the Output Enable ($\overline{OE}$) is HIGH, the outputs are in the high-impedance state. The latch operation is independent of the state of the Output Enable.

The CD54/74FCT373 and CD54/74FCT533 are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over two temperature ranges: Commercial (0 to 70°C) and Extended Industrial (-55 to +125°C).

The CD54FCT373 and CD54FCT533 are also available in chip form (H suffix). These unpackaged devices are operable over the -55 to +125°C temperature range.

Family Features:

- *SCR-Latchup-resistant CMOS process and circuit design*
- *Speed of bipolar FAST*/AS/S with significantly reduced power consumption*
- *48/32-mA output sink current (commercial/extended industrial)*
- *Output voltage swing limited to 3.7 V @ V_{CC} = 5 V*
- *Controlled output-edge rates*
- *Input/output isolation to V_{CC}*
- *BiMOS technology with low quiescent power*

*FAST is a Registered Trademark of Fairchild Semiconductor Corp.

TRUTH TABLE

Output Enable	Latch Enable	Data	FCT373 Output	FCT533 Output
L	H	H	H	L
L	H	L	L	H
L	L	l	L	H
L	L	h	H	L
H	X	X	Z	Z

Note:
L = Low voltage level
H = High voltage level
l = Low voltage level one set-up time prior to the high-to-low latch enable transition.
h = High voltage level one set-up time prior to the high-to-low latch enable transition.
X = Don't Care
Z = High Impedance State

Printed in USA/5-89

File Number **2230**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

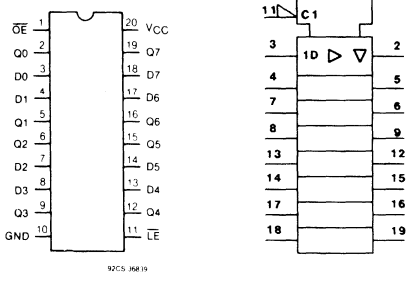
DC SUPPLY-VOLTAGE (V_{CC}) ..... -0.5 to 6 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ V) ..... -20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ V) ..... -50 mA
DC OUTPUT SINK CURRENT per Output Pin, I_O ..... +70 mA
DC OUTPUT SOURCE CURRENT per Outpin Pin, I_O ..... -30 mA
DC V_{CC} CURRENT (I_{CC}) ..... 140 mA
DC GROUND CURRENT (I_{GND}) ..... 400 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE E, M ..... -55 to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only ..... +300°C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V_{CC}*:			
CD74 Series, T_A = 0 to 70°C	4.75	5.25	V
CD54 Series, T_A = -55 to +125°C	4.5	5.5	V
DC Input Voltage, V_I	0	V_{CC}	V
DC Output Voltage, V_O	0	$\leq V_{CC}$	V
Operating Temperature, T_A	-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv	0	10	ns/V

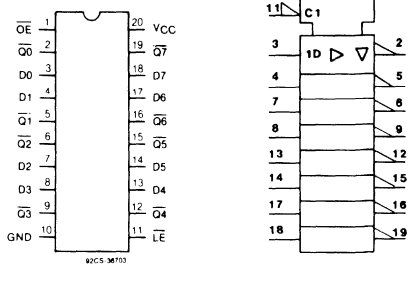
*Unless otherwise specified, all voltages are referenced to ground.

CD54/74FCT373



TERMINAL ASSIGNMENT **IEC LOGIC SYMBOL**

CD54/74FCT533



TERMINAL ASSIGNMENT **IEC LOGIC SYMBOL**

STATIC ELECTRICAL CHARACTERISTICS
FCT Series:

74FCT Commercial Temperature Range, 0 to 70°C. V_{CC} max = 5.25 V, V_{CC} min = 4.75 V

54FCT Extended Industrial Temperature Range, -55 to +125°C. V_{CC} max = 5.5 V, V_{CC} min = 4.5 V

CHARACTERISTICS		TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
					+25		0 to +70		-55 to +125		
		V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage	V_{IL}			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage	V_{OH}	V_{IH} or V_{IL}	-15	MIN.	2.4	—	2.4	—	—	—	V
			-12		2.4	—	—	—	2.4	—	
Low-Level Output Voltage	V_{OL}	V_{IH} or V_{IL}	48	MIN.	—	0.55	—	0.55	—	—	
			32		—	0.55	—	—	—	0.55	
High-Level Input Current	I_{IH}	V_{CC}		MAX.	—	0.1	—	1	—	1	μA
Low-Level Input Current	I_{IL}	GND		MAX.	—	-0.1	—	-1	—	-1	μA
3-State Leakage Current	I_{OZH}	V_{CC}		MAX.	—	0.5	—	10	—	10	μA
	I_{OZL}	GND		MAX.	—	-0.5	—	-10	—	-10	
Short-Circuit Output Current*	I_{OS}	V_{CC} or GND V_O = 0		MAX.	-60	—	-60	—	-60	—	mA
Input Clamp Voltage	V_{IK}	V_{CC} or GND	-18	MIN.	—	-1.2	—	-1.2	—	-1.2	V
Quiescent Supply Current, MSI	I_{CC}	V_{CC} or GND	0	MAX.	—	8	—	80	—	500	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load	ΔI_{CC}	3.4 †		MAX.	—	1.6	—	1.6	—	2	mA

*Not more than one output should be shorted at one time. Test duration should not exceed 100 ms.
†Inputs that are not measured are at V_{CC} or Gnd.

FCT Input Loading: All inputs are 1 unit load. Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 1.6 mA max. @ 70°C.

3

PREREQUISITE FOR SWITCHING:

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) -°C				UNITS
			0 to +70		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
$\overline{LE}$ Pulse Width	t_W	5†	6	—	6	—	ns
Setup Time Data to $\overline{LE}$	t_{SU}	5	2	—	2	—	ns
Hold Time Data to $\overline{LE}$	t_H	5	1.5	—	1.5	—	ns

†5 V: min. is @ 4.5 V
5 V: min. is @ 4.75 V for 0 to +70° C

SWITCHING CHARACTERISTICS: t_r, t_f = 2.5 ns, C_L = 50 pF, R_L — See Fig. 4

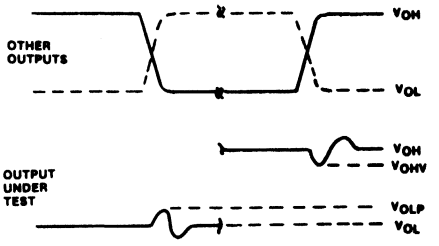
CHARACTERISTICS		SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) -°C				UNITS
				0 to +70		-55 to +125		
				MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Data to Outputs	373	t_{PLH}	5†	1.5	8	1.5	8.5	ns
	533	t_{PHL}		1.5	8	1.5	8.5	
$\overline{LE}$ to Outputs	373	t_{PLH}	5	2	13	2	15	ns
	533	t_{PHL}		2	13	2	14	
Output Enable Times	373	t_{PZL}	—	1.5	12	1.5	13.5	ns
	533	t_{PZH}	—	1.5	11	1.5	12.5	
Output Disable Times	373	t_{PLZ}	—	1.5	7.5	1.5	10	ns
	533	t_{PHZ}	—	1.5	7	1.5	8.5	
Power Dissipation Capacitance	373	C_{PD}§	—					pF
	533		—					
Min. (Valley) V_{OHV} During Switching of Other Outputs (Output Under Test Not Switching)		V_{OHV} See Fig. 1	5	0.5 Typ. @ 25°C				V
Max. (Peak) V_{OLP} During Switching of Other Outputs (Output Under Test Not Switching)		V_{OLP} See Fig. 1	5	1 Typ. @ 25°C				V
Input Capacitance		C_I	—	—	10	—	10	pF
3-State Output Capacitance		C_O	—	—	15	—	15	pF

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

5 V: min. is @ 5.25 V for 0 to +70°C
max. is @ 4.75 V for 0 to +70°C

§C_{PD}, measured per latch, is used to determine the dynamic power consumption.
P_D (per package) = $V_{CC}\, I_{cc} + \Sigma\, (V_{CC}^2\, f_i\, C_{PD} + V_O^2\, f_o\, C_L + V_{CC}\, \Delta I_{CC} D)$ where V_{cc} = supply voltage
ΔI_{CC} = flow through current x unit load
C_L = output load capacitance
D = duty cycle of input high
f_o = output frequency
f_i = input frequency

PARAMETER MEASUREMENT INFORMATION



NOTES:
1. V_{OLP} IS MEASURED WITH RESPECT TO A GROUND REFERENCE NEAR THE OUTPUT UNDER TEST. V_{OHV} IS MEASURED WITH RESPECT TO V_{OH}.
2. INPUT PULSES HAVE THE FOLLOWING CHARACTERISTICS: PRR ≤ 1 MHz, t_r = 3 ns, t_f = 3 ns, SKEW 1 ns.
3. R.F. FIXTURE WITH 700-MHz DESIGN RULES REQUIRED. IC SHOULD BE SOLDERED INTO TEST BOARD AND BYPASSED WITH 0.1 μF CAPACITOR. SCOPE AND PROBES REQUIRE 700-MHz BANDWIDTH.

92CS-42406R1

Fig. 1 - Simultaneous switching transient waveforms.

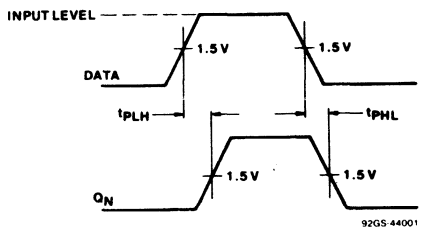


Fig. 2 - Data to Qn output propagation delays.

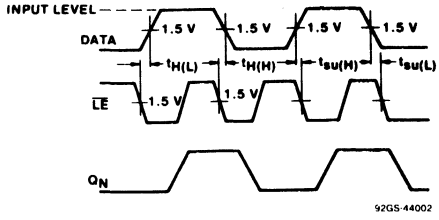
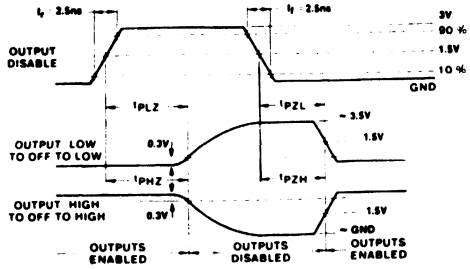
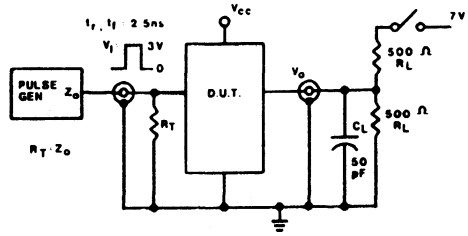


Fig. 3 - Latch Enable prerequisite times.





TEST	SWITCH POSITION
t_{PLZ} t_{PZL} OPEN DRAIN	CLOSED
t_{PHZ} t_{PZH} t_{PLH} t_{PHL}	OPEN

Fig. 4 - Three-state propagation delay times and test circuit.

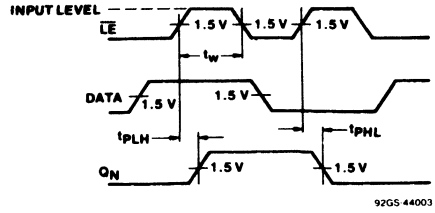
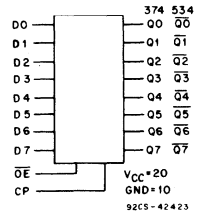


Fig. 5 - Latch Enable propagation delays.

CD54/74FCT374, CD54/74FCT534



FUNCTIONAL DIAGRAM

Octal D-Type Flip-Flops, 3-State

Positive-Edge Triggered

CD54/74FCT374 - Non-Inverting
CD54/74FCT534 - Inverting

Type Features:
- *Buffered inputs*
- *Typical propagation delay: 3.5 ns @ V_{CC} = 5 V, T_A = 25°C, C_L = 50 pF*

The CD54/74FCT374 and CD54/74FCT534 octal D-type, 3-state, positive-edge triggered flip-flops use a small-geometry BiMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output-HIGH level to two diode drops below V_{CC}. This resultant lowering of output swing (0 to 3.7 V) reduces power bus ringing (a source of EMI) and minimizes V_{CC} bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 32 to 48 milliamperes.

The eight flip-flops enter data into their registers on the LOW-to-HIGH transistion of the clock (CP). The Output Enable ($\overline{OE}$) controls the 3-state outputs and is independent of the register operation. When the Output Enable ($\overline{OE}$) is HIGH, the outputs are in the high-impedance state. The CD54/74FCT374 and CD54/74FCT534 share the same configurations, but the CD54/74FCT374 outputs are non-inverted while the CD54/74FCT534 devices have inverted outputs. (For flow-through pin configurations, see CD54/74FCT564 and CD54/74FCT574.)

The CD54/74FCT374 and CD54/74FCT534 are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over two temperature ranges: Commerical (0 to 70°C) and Extended Industrial (-55 to +125°C).

The CD54FCT374 and CD54FCT534 are also available in chip form (H suffix). These unpackaged devices are operable over the -55 to +125°C temperature range.

Family Features:
- *SCR-latchup-resistant CMOS process and circuit design*
- *Speed of bipolar FAST*/AS/S with significantly reduced power consumption*
- *48/32-mA output sink current (commercial/extended industrial)*
- *Output voltage swing limited to 3.7 V @ V_{CC} = 5 V*
- *Controlled output-edge rates*
- *Input/output isolation to V_{CC}*
- *BiMOS technology with low quiescent power*

*FAST is a Registered Trademark of Fairchild Semiconductor Corp.

TRUTH TABLE

INPUTS			OUTPUTS	
			374	534
$\overline{OE}$	CP	Dn	Qn	$\overline{Qn}$
L	_/‾	H	H	L
L	_/‾	L	L	H
L	L	X	Qo	$\overline{Qo}$
H	X	X	Z	Z

H = High level (steady state)
L = Low level (steady state)
X = Don't care
_/‾ = Transition from low to high level
Qo = The level of Q before the indicated steady-state input conditions were established
$\overline{Qo}$ = The level of $\overline{Q}$ before the indicated steady-state input conditions were established
Z = High impedance

Printed in USA/7-89

File Number **2305**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

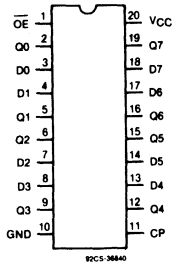
DC SUPPLY VOLTAGE (V_{CC}) ..... -0.5 to 6 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ V) ..... -20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ V) ..... -50 mA
DC OUTPUT SINK CURRENT per Output Pin, I_O ..... +70 mA
DC OUTPUT SOURCE CURRENT per Output Pin, I_O ..... -30 mA
DC V_{CC} CURRENT (I_{CC}) ..... 140 mA
DC GROUND CURRENT (I_{GND}) ..... 400 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE E, M ..... -55 to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only ..... +300°C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

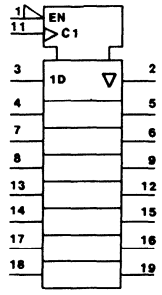
CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V_{CC}*:			
CD74 Series, T_A = 0 to 70°C	4.75	5.25	V
CD54 Series, T_A = -55 to +125°C	4.5	5.5	
DC Input Voltage, V_I	0	V_{CC}	
DC Output Voltage, V_O	0	$\leq V_{CC}$	
Operating Temperature, T_A	-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv	0	10	ns/V

*Unless otherwise specified, all voltages are referenced to ground.

CD54/74FCT374

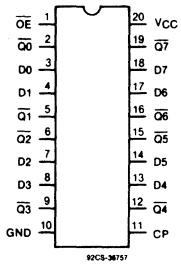


TERMINAL ASSIGNMENT

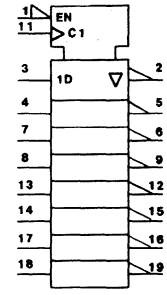


IEC LOGIC SYMBOL

CD54/74FCT534



TERMINAL ASSIGNMENT



IEC LOGIC SYMBOL

STATIC ELECTRICAL CHARACTERISTICS
FCT Series:
74FCT Commercial Temperature Range, 0 to 70°C; V_{CC} max = 5.25 V, V_{CC} min = 4.75 V
54FCT Extended Industrial Temperature Range, -55 to +125°C; V_{CC} max = 5.5 V, V_{CC} min = 4.5 V

CHARACTERISTICS		TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
					+25		0 to +70		-55 to +125		
		V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage	V_{IL}			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage	V_{OH}	V_{IH} or V_{IL}	-15	MIN.	2.4	—	2.4	—	—	—	V
			-12		2.4	—	—	—	2.4	—	
Low-Level Output Voltage	V_{OL}	V_{IH} or V_{IL}	48	MIN.	—	0.55	—	0.55	—	—	
			32		—	0.55	—	—	—	0.55	
High-Level Input Current	I_{IH}	V_{CC}		MAX.	—	0.1	—	1	—	1	μA
Low-Level Input Current	I_{IL}	GND		MAX.	—	-0.1	—	-1	—	-1	μA
3-State Leakage Current	I_{OZH}	V_{CC}		MAX.	—	0.5	—	10	—	10	μA
	I_{OZL}	GND		MAX.	—	-0.5	—	-10	—	-10	
Short-Circuit Output Current*	I_{OS}	V_{CC} or GND V_O = 0		MAX.	-60	—	-60	—	-60	—	mA
Input Clamp Voltage	V_{IK}	V_{CC} or GND	-18	MIN.	—	-1.2	—	-1.2	—	-1.2	V
Quiescent Supply Current, MSI	I_{CC}	V_{CC} or GND	0	MAX.	—	8	—	80	—	500	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load	ΔI_{CC}	3.4 V†		MAX.	—	1.6	—	1.6	—	2	mA

*Not more than one output should be shorted at one time. Test duration should not exceed 100 ms.
†Inputs that are not measured are at V_{CC} or Gnd.

FCT Input Loading: All inputs are 1 unit load. Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 1.6 mA max. @ 70°C.

PREREQUISITE FOR SWITCHING:

CHARACTERISTICS		SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) -°C				UNITS
				0 to +70		-55 to +125		
				MIN.	MAX.	MIN.	MAX.	
Clock Pulse Width		t_w	5†	7	—	7	—	ns
Setup Time Data to Clock		t_{su}	5	2	—	2.5	—	ns
Hold Time Data to Clock	374	t_H	5	2		2		ns
	534			1.5		1.5		
Maximum Clock Frequency		f_{MAX}	5	70	—	60	—	MHz

†5 V: min. is @ 4.5 V
5 V: min. is @ 4.75 V for 0 to +70°C

SWITCHING CHARACTERISTICS: t_r, t_f = 2.5 ns, C_L = 50 pF, R_L - See Fig. 4

CHARACTERISTICS		SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) -°C				UNITS
				0 to +70		-55 to +125		
				MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Clock to Q	374	t_{PLH} t_{PHL}	5†	2	10	2	11	ns
Clock to $\overline{Q}$	534	t_{PLH} t_{PHZ}	5	1.5	10	1.5	11	ns
Output Enable and Disable to Q	374	t_{PLZ} t_{PHZ}	5	1.5	8	1.5	8	ns
		t_{PZL} t_{PZH}	5	1.5	12.5	1.5	14	
Output Enable and Disable to $\overline{Q}$	534	t_{PLZ} t_{PHZ}	5	1.5	8	1.5	8	ns
		t_{PZL} t_{PZH}	5	1.5	12.5	1.5	14	
Power Dissipation Capacitance		C_{PD}§	—					pF
Min. (Valley) V_{OHV} During Switching of Other Outputs (Output Under Test Not Switching)		V_{OHV} See Fig. 1	5	0.5 Typ. @ 25°C				V
Max. (Peak) V_{OLP} During Switching of Other Outputs (Output Under Test Not Switching)		V_{OLP} See Fig. 1	5	1 Typ. @ 25°C				V
Input Capacitance		C_I	—	—	10	—	10	pF
3-State Output Capacitance		C_O	—	—	15	—	15	pF

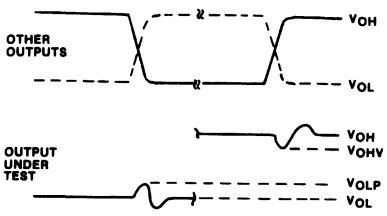
†5 V: min. is @ 5.5 V
max. is @ 4.5 V

5 V: min. is @ 5.25 V for 0 to +70°C
max. is @ 4.75 V for 0 to +70°C

§C_{PD}, measured per flip-flop, is used to determine the dynamic power consumption.
P_D (per package) = V_{CC} I_{CC} + Σ (V_{CC}^2 f_i C_{PD} + V_o^2 f_o C_L + V_{CC} ΔI_{CC}D)
where V_{CC} = supply voltage
ΔI_{CC} = flow-through current x unit load
C_L = output load capacitance
D = duty cycle of input high
f_o = output frequency
f_i = input frequency

3

PARAMETER MEASUREMENT INFORMATION



NOTES:
1. V_{OLP} IS MEASURED WITH RESPECT TO A GROUND REFERENCE NEAR THE OUTPUT UNDER TEST. V_{OHV} IS MEASURED WITH RESPECT TO V_{OH}.
2. INPUT PULSES HAVE THE FOLLOWING CHARACTERISTICS: PRR ≤ 1 MHz, t_r = 3 ns, t_f = 3 ns, SKEW 1 ns.
3. R.F. FIXTURE WITH 700-MHz DESIGN RULES REQUIRED. IC SHOULD BE SOLDERED INTO TEST BOARD AND BYPASSED WITH 0.1 μF CAPACITOR. SCOPE AND PROBES REQUIRE 700-MHz BANDWIDTH.

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Fig. 1 - Simultaneous switching transient waveforms.

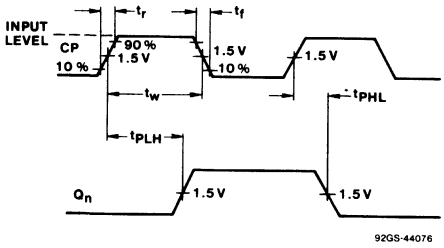


Fig. 2 - Propagation delay times.

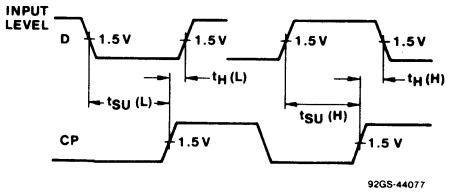
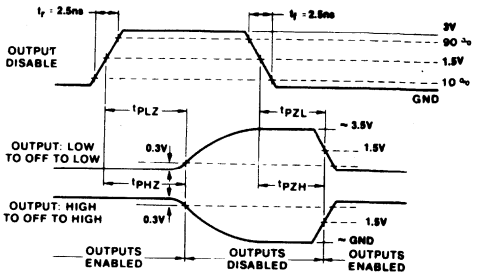
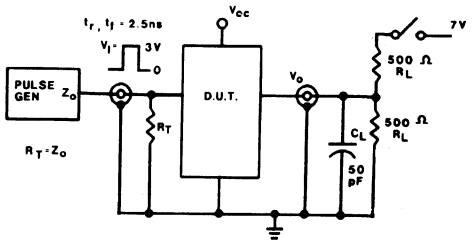


Fig. 3 - Setup and hold times.

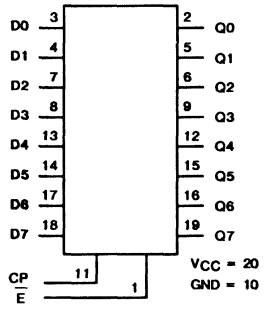




TEST	SWITCH POSITION
t_{PLZ} t_{PZL} OPEN DRAIN	CLOSED
t_{PHZ} t_{PZH} t_{PLH} t_{PHL}	OPEN

Fig. 4 - Three-state propagation delay times and test circuit.

CD54/74FCT377



FUNCTIONAL DIAGRAM

Octal D-Type Flip-Flop with Data Enable

Type Features:

- *Buffered inputs*
- *Typical propagation delay: 3.5ns @ V_{CC} = 5V, T_A = +25°C, C_L = 50pF*

3

The CD54/74FCT377 uses a small-geometry BiMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output-HIGH level to two diode drops below V_{CC}. This resultant lowering of output swing (0V to 3.7V) reduces power bus ringing (a source of EMI) and minimizes V_{CC} bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 32 to 48 milliamperes.

The CD54/74FCT377 is an octal D-type flip-flop with a buffered clock (CP) common to all eight flip-flops. All the flip-flops are loaded simultaneously on the positive edge of the clock (CP) when the Data Enable ($\overline{E}$) is LOW.

The CD54/74FCT377 is supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over two temperature ranges: Commercial (0°C to +70°C) and Extended Industrial (-55°C to +125°C).

The CD54FCT377 is also available in chip form (H suffix). These unpackaged devices are operable over the -55°C to +125°C temperature range.

Family Features:

- *SCR-latchup-resistant CMOS process and circuit design*
- *Speed of bipolar FAST*/AS/S with significantly reduced power consumption*
- *48/32-mA output sink current (commercial/extended industrial)*
- *Output voltage swing limited to 3.7V @ V_{CC} = 5V*
- *Controlled output-edge rates*
- *Input/output isolation to V_{CC}*
- *BiMOS technology with low quiescent power*

* FAST is a registered trademark of Fairchild Semiconductor Corp.

TRUTH TABLE

OPERATING MODE	INPUTS			OUTPUTS
	CP	$\overline{E}$	D_n	Q_n
Load "1"	⎍	l	h	H
Load "0"	⎍	l	l	L
Hold (do nothing)	⎍	h	X	no change
	X	H	X	no change

H = HIGH voltage level steady state.
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
L = LOW voltage level steady state
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
X = Immaterial
⎍ = LOW-to-HIGH clock transition.

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File Number **2388**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

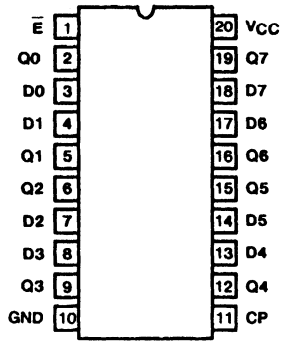
DC SUPPLY-VOLTAGE (V_{CC}) ..... -0.5V to 6V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5V$) ..... -20mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5V$) ..... -50mA
DC OUTPUT SINK CURRENT per Output Pin, I_O ..... +70mA
DC OUTPUT SOURCE CURRENT per Output Pin, I_O ..... -30mA
DC V_{CC} CURRENT (I_{CC}) 140mA
DC GROUND CURRENT (I_{GND}) 400mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55°C to +100°C (PACKAGE TYPE E) 500mW
For T_A = +100°C to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8mW/°C to 300mW
For T_A = -55°C to +70°C (PACKAGE TYPE M) 400mW
For T_A = +70°C to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6mW/°C to 70mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE E, M ..... -55°C to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 in. ± 1/32 in. (1.59mm ± 0.79mm) from case for 10s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59mm) with solder contacting lead tips only ..... +300°C

RECOMMENDED OPERATING CONDITIONS:

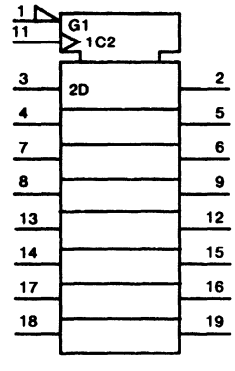
The following are normal operating ranges for these devices. For maximum reliability, devices should always be operated within these ranges.

CHARACTERISTIC		LIMITS MIN	LIMITS MAX	UNITS
Supply-Voltage Range, V_{CC}*:	CD74 Series, T_A = 0°C to 70°C	4.75	5.25	V
	CD54 Series, T_A = -55°C to +125°C	4.5	5.5	V
DC Input Voltage, V_I		0	V_{CC}	V
DC Output Voltage, V_O		0	$\leq V_{CC}$	V
Operating Temperature, T_A		-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv		0	10	ns/V

* Unless otherwise specified, all voltages are referenced to ground.



TERMINAL ASSIGNMENT



IEC LOGIC SYMBOL

STATIC ELECTRICAL CHARACTERISTICS

FCT Series: 74FCT Commercial Temperature Range, 0°C to +70°C; V_{CC} max = 5.25V, V_{CC} min = 4.75V
54FCT Extended Industrial Temperature Range, -55°C to +125°C; V_{CC} max = 5.5V, V_{CC} min = 4.5V

CHARACTERISTICS		TEST CONDITIONS V_I (V)	TEST CONDITIONS I_O (mA)	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) +25°C MIN	+25°C MAX	0°C to +70°C MIN	0°C to +70°C MAX	-55°C to +125°C MIN	-55°C to +125°C MAX	UNITS
High-Level Input Voltage	V_{IH}			4.5 to 5.5	2	-	2	-	2	-	V
Low-Level Input Voltage	V_{IL}			4.5 to 5.5	-	0.8	-	0.8	-	0.8	V
High-Level Output Voltage	V_{OH}	V_{IH} or	-15	MIN	2.4	-	2.4	-	-	-	V
		V_{IL}	-12	MIN	2.4	-	-	-	2.4	-	V
Low-Level Output Voltage	V_{OL}	V_{IH} or	48	MIN	-	0.55	-	0.55	-	-	V
		V_{IL}	32	MIN	-	0.55	-	-	-	0.55	V
High-Level Input Current	I_{IH}	V_{CC}		MAX	-	0.1	-	1	-	1	µA
Low-Level Input Current	I_{IL}	GND		MAX	-	-0.1	-	-1	-	-1	µA
3-State Leakage Current	I_{OZH}	V_{CC}		MAX	-	0.5	-	10	-	10	µA
	I_{OZL}	GND		MAX	-	-0.5	-	-10	-	-10	µA
Short-Circuit Output Current *	I_{OS}	V_{CC} or GND $V_O = 0$		MAX	-60	-	-60	-	-60	-	mA
Input Clamp Voltage	V_{IK}	V_{CC} or GND	-18	MIN	-	-1.2	-	-1.2	-	-1.2	V
Quiescent Supply Current, MSI	I_{CC}	V_{CC} or GND	0	MAX	-	8	-	80	-	500	µA
Additional Quiescent Supply Current per Input Pin TTL Inputs High, 1 Unit Load	ΔI_{CC}	3.4V†		MAX	-	1.6	-	1.6	-	2	mA

* Not more than one output should be shorted at one time. Test duration should not exceed 100ms.
† Inputs that are not measured are at V_{CC} or GND.

FCT Input Loading: All inputs are 1 unit load. Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 1.6mA max. @ +70°C.

3

PREREQUISITE FOR SWITCHING

CHARACTERISTICS		SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) 0°C to +70°C MIN	0°C to +70°C MAX	-55°C to +125°C MIN	-55°C to +125°C MAX	UNITS
CP Pulse Width		t_W	5†	7	-	7	-	ns
Setup Time	D_n to CP	t_{SU}	5	2.5	-	3	-	ns
	$\overline{E}$ to CP	t_{SU}	5	3	-	3	-	ns
Hold Time	D_n to CP	t_H	5	2	-	2.5	-	ns
	$\overline{E}$ to CP	t_H	5	4	-	5	-	ns
Maximum Clock Frequency		f_{MAX}	5	70	-	70	-	MHz

†5V: min. is @ 4.5V
5V: min. is @ 4.75V for 0°C to +70°C

SWITCHING CHARACTERISTICS: t_r, t_f = 2.5ns, C_L = 50pF, R_L = 500Ω

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) 0°C to +70°C MIN	0°C to +70°C MAX	-55°C to +125°C MIN	-55°C to +125°C MAX	UNITS
Propagation Delays: CP to Q_n	t_{PLH}, t_{PHL}	5†	2	13	2	15	ns
Power Dissipation Capacitance	C_{PD}§	-					pF
Input Capacitance	C_I	-	-	10	-	10	pF

†5V: min. is @ 5.5V
max. is @ 4.5V
5V: min. is @ 5.25V for 0°C to +70°C
max. is @ 4.75V for 0°C to +70°C

§C_{PD}, measured per flip-flop, is used to determine the dynamic power consumption.
P_D (per package) = $V_{CC} I_{CC} + \Sigma (V_{CC}^2 f_i C_{PD} + V_O^2 f_o C_L + V_{CC} \Delta I_{CC} D)$ where:
V_{CC} = supply voltage
ΔI_{CC} = flow through current x unit load
C_L = output load capacitance
D = duty cycle of input high
f_o = output frequency
f_i = input frequency

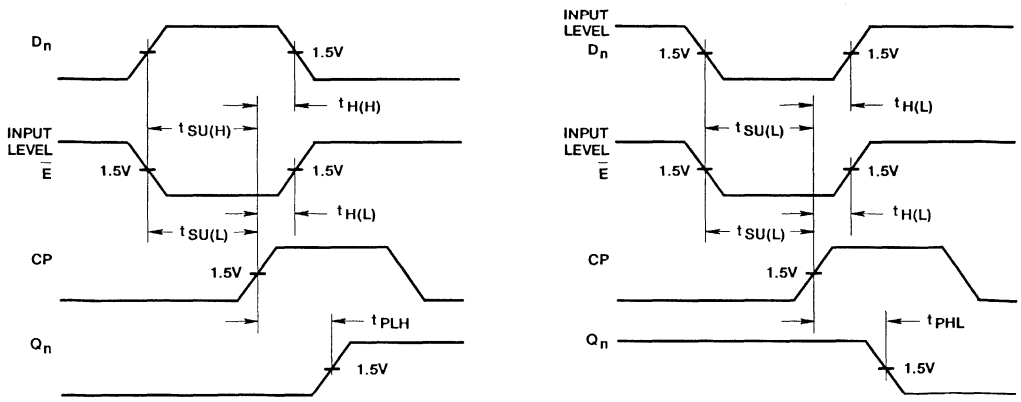
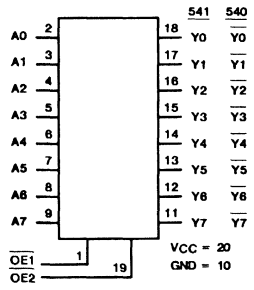


Figure 2 - Setup and hold times and propagation delay times.

CD54/74FCT540, CD54/74FCT541

Advance Information



FUNCTIONAL DIAGRAM

Octal Buffers/Line Drivers, 3-State

CD54/74FCT540 - Inverting
CD54/74FCT541 - Non-Inverting

Type Features:

- *Buffered inputs*
- *Typical propagation delay: 3ns @ V_{CC} = 5V, T_A = +25°C, C_L = 50pF*

3

The CD54/74FCT540 and CD54/74FCT541 octal buffers/line drivers use a small-geometry BiMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output-HIGH level to two diode drops below V_{CC}. This resultant lowering of output swing (0V to 3.7V) reduces power bus ringing (a source of EMI) and minimizes V_{CC} bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 48 to 64 milliamperes.

The CD54/74FCT540 is a 3-state buffer having two active-LOW output enables. The CD54/74FCT541 is a non-inverting 3-state buffer having two active-LOW output enables.

The CD54/74FCT540 and CD54/74FCT541 are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over two temperature ranges: Commercial (0°C to +70°C) and Extended Industrial (-55°C to +125°C).

The CD54FCT540 and CD54FCT541 are also available in chip form (H suffix). These unpackaged devices are operable over the -55°C to +125°C temperature range.

Family Features:

- *SCR-latchup-resistant CMOS process and circuit design*
- *Speed of bipolar FAST*/AS/S with significantly reduced power consumption*
- *64/48-mA output sink current (commercial/extended industrial)*
- *Output voltage swing limited to 3.7V @ V_{CC} = 5V*
- *Controlled output-edge rates*
- *Input/output isolation to V_{CC}*
- *BiMOS technology with low quiescent power*

* FAST is a registered trademark of Fairchild Semiconductor Corp.

TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{OE1}$	$\overline{OE2}$	A_n	FCT540	FCT541
L	L	H	L	H
H	X	X	Z	Z
X	H	X	Z	Z
L	L	L	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = HIGH Impedance

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File Number **2383**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (V_{CC}) ..... -0.5V to 6V
DC INPUT DIODE CURRENT, I_{IK} (for V_I < -0.5V) ..... -20mA
DC OUTPUT DIODE CURRENT, I_{OK} (for V_O < -0.5V) ..... -50mA
DC OUTPUT SINK CURRENT per Output Pin, I_O ..... +70mA
DC OUTPUT SOURCE CURRENT per Output Pin, I_O ..... -30mA
DC V_{CC} CURRENT (I_{CC}) 140mA
DC GROUND CURRENT (I_{GND}) 528mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55°C to +100°C (PACKAGE TYPE E) 500mW
For T_A = +100°C to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8mW/°C to 300mW
For T_A = -55°C to +70°C (PACKAGE TYPE M) 400mW
For T_A = +70°C to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6mW/°C to 70mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE E, M ..... -55°C to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 in. ± 1/32 in. (1.59mm ± 0.79mm) from case for 10s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59mm) with solder contacting lead tips only ..... +300°C

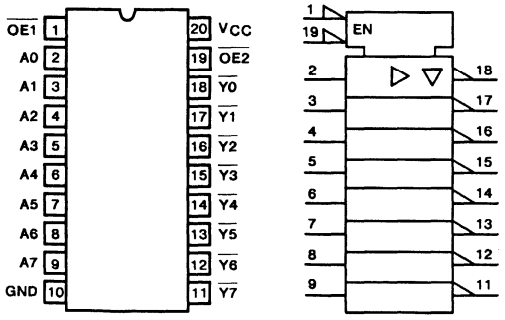
RECOMMENDED OPERATING CONDITIONS:

The following are normal operating ranges for these devices. For maximum reliability, devices should always be operated within these ranges.

CHARACTERISTIC		LIMITS MIN	LIMITS MAX	UNITS
Supply-Voltage Range, V_{CC}*:	CD74 Series, T_A = 0°C to 70°C	4.75	5.25	V
	CD54 Series, T_A = -55°C to +125°C	4.5	5.5	V
DC Input Voltage, V_I		0	V_{CC}	V
DC Output Voltage, V_O		0	$\leq V_{CC}$	V
Operating Temperature, T_A		-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv		0	10	ns/V

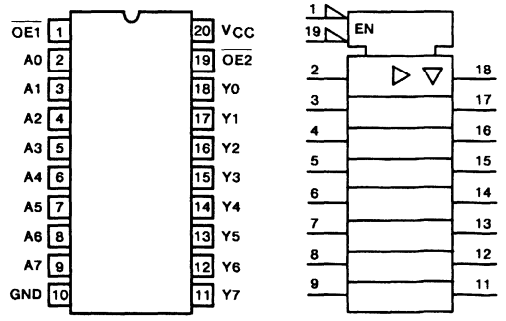
* Unless otherwise specified, all voltages are referenced to ground.

CD54/74FCT540 TYPES



TERMINAL ASSIGNMENT — IEC LOGIC SYMBOL

CD54/74FCT541 TYPES



TERMINAL ASSIGNMENT — IEC LOGIC SYMBOL

STATIC ELECTRICAL CHARACTERISTICS

FCT Series: 74FCT Commercial Temperature Range, 0°C to +70°C; V_{CC} max = 5.25V, V_{CC} min = 4.75V
54FCT Extended Industrial Temperature Range, -55°C to +125°C; V_{CC} max = 5.5V, V_{CC} min = 4.5V

CHARACTERISTICS		TEST CONDITIONS			AMBIENT TEMPERATURE (T_A)						UNITS
					+25°C		0°C to +70°C		-55°C to +125°C		
		V_I (V)	I_O (mA)	V_{CC} (V)	MIN	MAX	MIN	MAX	MIN	MAX	
High-Level Input Voltage	V_{IH}			4.5 to 5.5	2	-	2	-	2	-	V
Low-Level Input Voltage	V_{IL}			4.5 to 5.5	-	0.8	-	0.8	-	0.8	V
High-Level Output Voltage	V_{OH}	V_{IH} or	-15	MIN	2.4	-	2.4	-	-	-	V
		V_{IL}	-12	MIN	2.4	-	-	-	2.4	-	V
Low-Level Output Voltage	V_{OL}	V_{IH} or	64	MIN	-	0.55	-	0.55	-	-	V
		V_{IL}	48	MIN	-	0.55	-	-	-	0.55	V
High-Level Input Current	I_{IH}	V_{CC}		MAX	-	0.1	-	1	-	1	µA
Low-Level Input Current	I_{IL}	GND		MAX	-	-0.1	-	-1	-	-1	µA
3-State Leakage Current	I_{OZH}	V_{CC}		MAX	-	0.5	-	10	-	10	µA
	I_{OZL}	GND		MAX	-	-0.5	-	-10	-	-10	µA
Short-Circuit Output Current *	I_{OS}	V_{CC} or GND $V_O = 0$		MAX	-60	-	-60	-	-60	-	mA
Input Clamp Voltage	V_{IK}	V_{CC} or GND	-18	MIN	-	-1.2	-	-1.2	-	-1.2	V
Quiescent Supply Current, MSI	I_{CC}	V_{CC} or GND	0	MAX	-	8	-	80	-	500	µA
Additional Quiescent Supply Current per Input Pin TTL Inputs High, 1 Unit Load	ΔI_{CC}	3.4V†		MAX	-	1.6	-	1.6	-	2	mA

* Not more than one output should be shorted at one time. Test duration should not exceed 100ms.
† Inputs that are not measured are at V_{CC} or GND.

FCT Input Loading: All inputs are 1 unit load. Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 1.6mA max. @ +70°C.

3

SWITCHING CHARACTERISTICS

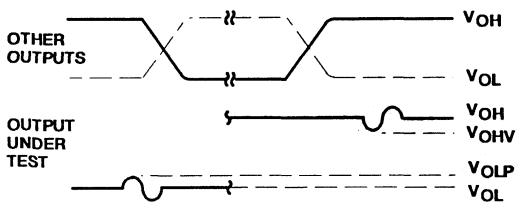
FCT Series: t_r, t_f = 2.5ns, C_L = 50pF, R_L - See Figure 3

CHARACTERISTICS		SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) 0°C to +70°C MIN	0°C to +70°C MAX	-55°C to +125°C MIN	-55°C to +125°C MAX	UNITS
Propagation Delays: Data to Outputs	FCT540	t_{PLH}, t_{PHL}	5†	2	8.5	2	9.5	ns
	FCT541	t_{PLH}, t_{PHL}	5†	2	8	2	9	ns
Output Disable to Output		t_{PLZ}, t_{PHZ}	5	2	9.5	2	12.5	ns
Output Enable to Output		t_{PZH}, t_{PZL}	5	2	10	2	10.5	ns
Power Dissipation Capacitance		C_{PD}§	-					pF
Min. (Valley) V_{OHV} During Switching of Other Outputs (Output Under Test Not Switching)		V_{OHV} See Figure 1	5	0.5 Typical @ +25°C				V
Max. (Peak) V_{OLP} During Switching of Other Outputs (Output Under Test Not Switching)		V_{OLP} See Figure 1	5	1 Typical @ +25°C				V
Input Capacitance		C_I	-	-	10	-	10	pF
3-State Output Capacitance		C_O	-	-	15	-	15	pF

†5V: min. is @ 5.5V
max. is @ 4.5V
5V: min. is @ 5.25V for 0°C to +70°C
max. is @ 4.75V for 0°C to +70°C

§C_{PD}, measured per function, is used to determine the dynamic power consumption.
P_D (per package) = V_{CC} I_{CC} + Σ (V_{CC}^2 f_i C_{PD} + V_O^2 f_o C_L + V_{CC} ΔI_{CC} D) where:
V_{CC} = supply voltage
ΔI_{CC} = flow through current x unit load
C_L = output load capacitance
D = duty cycle of input high
f_o = output frequency
f_i = input frequency

PARAMETER MEASUREMENT INFORMATION



NOTES:
1. V_{OLP} is measured with respect to a ground reference near the output under test. V_{OHV} is measured with respect to V_{OH}.
2. Input pulses have the following characteristics: PRR ≤ 1MHz, t_r = 2.5ns, t_f = 2.5ns, skew 1ns.
3. R.F. fixture with 700-MHz design rules required. IC should be soldered into test board and bypassed with 0.1μF capacitor. Scope and probes require 700-MHz bandwidth.

Figure 1 - Simultaneous switching transient waveforms.

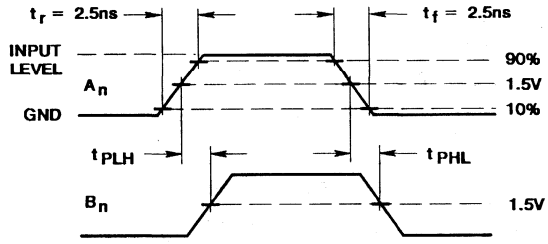
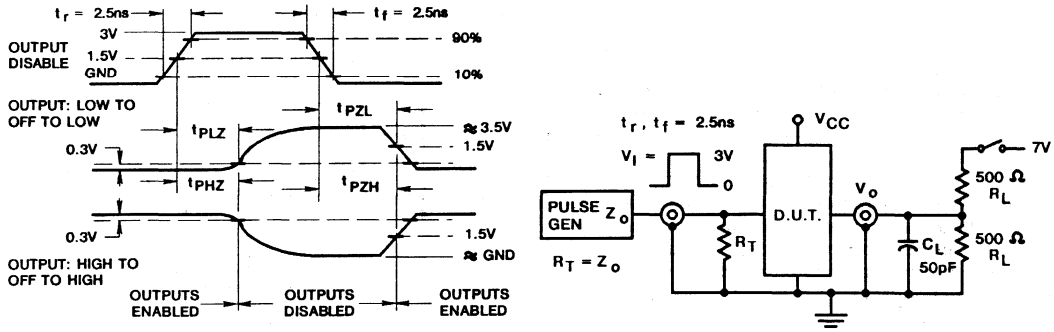


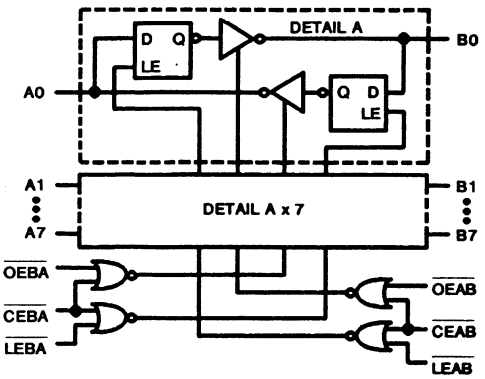
Figure 2 - Propagation delay times.



TEST	SWITCH POSITION
t_{PLZ}, t_{PZL}, OPEN DRAIN	CLOSED
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	OPEN

Figure 3 - Three-state propagation delay times and test circuit.

CD54/74FCT543, CD54/74FCT544



CD54/74FCT543 FUNCTIONAL DIAGRAM

Octal Register-Transceivers, 3-State

CD54/74FCT543 - Non-Inverting
CD54/74FCT544 - Inverting

Type Features:

- *Buffered inputs*
- *Typical propagation delay: 3.5ns @ VCC = 5V, TA = +25°C, CL = 50pF*

The CD54/74FCT543 and CD54/74FCT544 3-State octal register-transceviers use a small-geometry BiMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output-HIGH level to two diode drops below VCC. This resultant lowering of output swing (0V to 3.7V) reduces power bus ringing (a source of EMI) and minimizes VCC bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 48 to 64 milliamperes.

These devices contain two sets of eight D-type latches with separate input and output controls for each set. For data flow from A to B, for example, the A-to-B Enable ($\overline{CEAB}$) input must be LOW in order to enter data from A0-A7 or to take data from B0-B7, as indicated in the Truth Table. With $\overline{CEAB}$ LOW, a LOW signal on the A-to-B Latch Enable ($\overline{LEAB}$) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the $\overline{LEAB}$ signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{CEAB}$ and $\overline{OEAB}$ both LOW, the 3-state B output buffers are active and reflect the data present at the outut of the A latches. Control of data from B to A is similar, but uses the $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$ inputs.

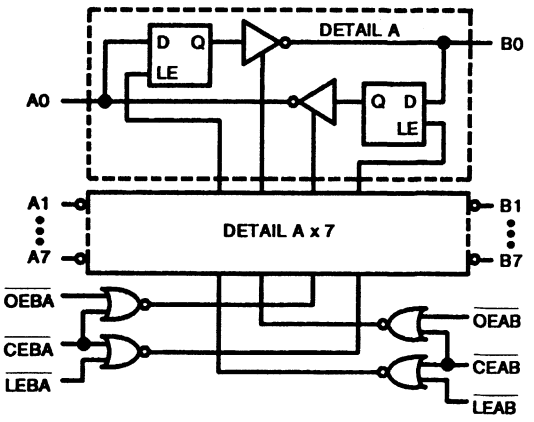
The CD54/74FCT543 and CD54/74FCT544 are supplied in 24-lead dual-in-line narrow-body plastic packages (EN suffix) and in 24-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over two temperature ranges: Commercial (0°C to +70°C) and Extended Industrial (-55°C to +125°C).

The CD54FCT543 and CD54FCT544 are also available in chip form (H suffix). These unpackaged devices are operable over the -55°C to +125°C temperature range.

Family Features:

- *SCR-latchup-resistant CMOS process and circuit design*
- *Speed of bipolar FAST*/AS/S with significantly reduced power consumption*
- *64/48-mA output sink current (commercial/extended industrial)*
- *Output voltage swing limited to 3.7V @ VCC = 5V*
- *Controlled output-edge rates*
- *Input/output isolation to VCC*
- *BiMOS technology with low quiescent power*

* FAST is a registered trademark of Fairchild Semiconductor Corp.



CD54/74FCT544 FUNCTIONAL DIAGRAM

Printed in USA/8-89

File Number 2399

TRUTH TABLE For A-to-B (Symmetric with B-to-A)

INPUTS			LATCH STATUS	OUTPUT BUFFERS
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A-TO-B	B0-B7
H	X	X	Storing	High Z
X	H	-	Storing	-
X	-	H	-	High Z
L	L	L	Transparent	Current A Inputs
L	H	L	Storing	Previous* A Inputs

* Before $\overline{LEAB}$ LOW-to-HIGH Transition
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
A-to-B data flow shown: B-to-A flow control is the same, except using $\overline{CEBA}$, $\overline{LEBA}$ and $\overline{OEBA}$

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (VCC) ..... -0.5V to 6V
DC INPUT DIODE CURRENT, IIK (for VI < -0.5V) ..... -20mA
DC OUTPUT DIODE CURRENT, IOK (for VO < -0.5V) ..... -50mA
DC OUTPUT SINK CURRENT per Output Pin, IO ..... +70mA
DC OUTPUT SOURCE CURRENT per Output Pin, IO ..... -30mA
DC VCC CURRENT (ICC) 140mA
DC GROUND CURRENT (IGND) 528mA
POWER DISSIPATION PER PACKAGE (PD):
For TA = -55°C to +100°C (PACKAGE TYPE E) 500mW
For TA = +100°C to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8mW/°C to 300mW
For TA = -55°C to +70°C (PACKAGE TYPE M) 400mW
For TA = +70°C to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6mW/°C to 70mW
OPERATING-TEMPERATURE RANGE (TA):
PACKAGE TYPE E, M ..... -55°C to +125°C
STORAGE TEMPERATURE (Tstg) ..... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 in. ± 1/32 in. (1.59mm ± 0.79mm) from case for 10s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59mm) with solder contacting lead tips only ..... +300°C

RECOMMENDED OPERATING CONDITIONS:

The following are normal operating ranges for these devices. For maximum reliability, devices should always be operated within these ranges.

CHARACTERISTIC		LIMITS MIN	LIMITS MAX	UNITS
Supply-Voltage Range, VCC*:	CD74 Series, TA = 0°C to 70°C	4.75	5.25	V
	CD54 Series, TA = -55°C to +125°C	4.5	5.5	V
DC Input Voltage, VI		0	VCC	V
DC Output Voltage, VO		0	≤VCC	V
Operating Temperature, TA		-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv		0	10	ns/V

* Unless otherwise specified, all voltages are referenced to ground.

STATIC ELECTRICAL CHARACTERISTICS

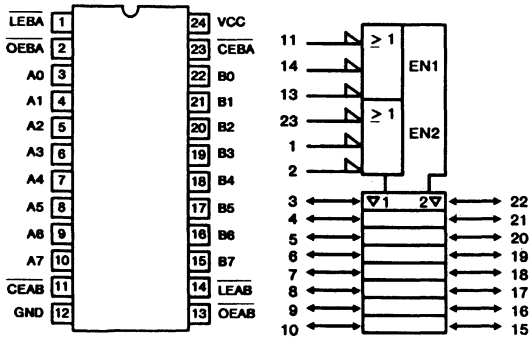
FCT Series: 74FCT Commercial Temperature Range, 0°C to +70°C; VCC max = 5.25V, VCC min = 4.75V
54FCT Extended Industrial Temperature Range, -55°C to +125°C; VCC max = 5.5V, VCC min = 4.5V

CHARACTERISTICS		TEST CONDITIONS VI (V)	TEST CONDITIONS IO (mA)	VCC (V)	AMBIENT TEMPERATURE (TA) +25°C MIN	+25°C MAX	0°C to +70°C MIN	0°C to +70°C MAX	-55°C to +125°C MIN	-55°C to +125°C MAX	UNITS
High-Level Input Voltage	VIH			4.5 to 5.5	2	-	2	-	2	-	V
Low-Level Input Voltage	VIL			4.5 to 5.5	-	0.8	-	0.8	-	0.8	V
High-Level Output Voltage	VOH	VIH or	-15	MIN	2.4	-	2.4	-	-	-	V
		VIL	-12	MIN	2.4	-	-	-	2.4	-	V
Low-Level Output Voltage	VOL	VIH or	64	MIN	-	0.55	-	0.55	-	-	V
		VIL	48	MIN	-	0.55	-	-	-	0.55	V
High-Level Input Current	IIH	VCC		MAX	-	0.1	-	1	-	1	µA
Low-Level Input Current	IIL	GND		MAX	-	-0.1	-	-1	-	-1	µA
3-State Leakage Current	IOZH	VCC		MAX	-	0.5	-	10	-	10	µA
	IOZL	GND		MAX	-	-0.5	-	-10	-	-10	µA
Short-Circuit Output Current *	IOS	VCC or GND VO = 0		MAX	-60	-	-60	-	-60	-	mA
Input Clamp Voltage	VIK	VCC or GND	-18	MIN	-	-1.2	-	-1.2	-	-1.2	V
Quiescent Supply Current, MSI	ICC	VCC or GND	0	MAX	-	8	-	80	-	500	µA
Additional Quiescent Supply Current per Input Pin TTL Inputs High, 1 Unit Load	ΔICC	3.4V†		MAX	-	1.6	-	1.6	-	2	mA

* Not more than one output should be shorted at one time. Test duration should not exceed 100ms.
† Inputs that are not measured are at VCC or GND.

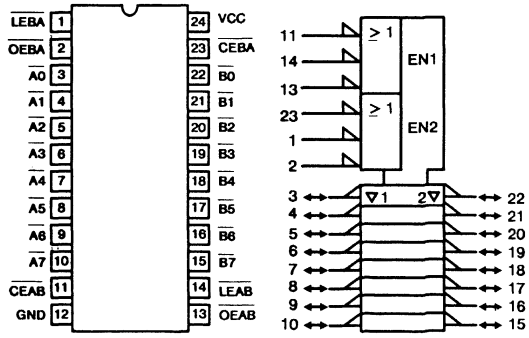
FCT Input Loading: All inputs are 1 unit load. Unit load is ΔICC limit specified in Static Characteristics Chart, e.g., 1.6mA max. @ +70°C.

CD54/74FCT543 TYPES



TERMINAL ASSIGNMENT — IEC LOGIC SYMBOL

CD54/74FCT544 TYPES



TERMINAL ASSIGNMENT — IEC LOGIC SYMBOL

PREREQUISITE FOR SWITCHING

CHARACTERISTICS		SYMBOL	VCC (V)	AMBIENT TEMPERATURE (TA) 0°C to +70°C MIN	MAX	-55°C to +125°C MIN	MAX	UNITS
Latch Enable Pulse Width	FCT543	tW	5†	9	-	9	-	ns
	FCT544	tW	5	7.5	-	9	-	ns
Data to Latch Enable Setup Time		tSU	5	3	-	3	-	ns
Data to Latch Enable Hold Time		tH	5	3	-	3	-	ns

†5V: min. is @ 4.5V
5V: min. is @ 4.75V for 0°C to +70°C

SWITCHING CHARACTERISTICS

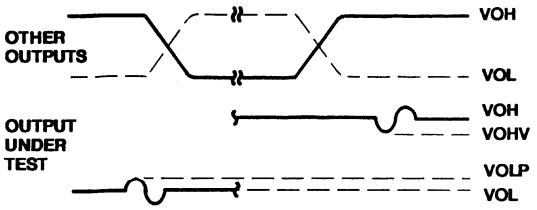
FCT Series: tr, tf = 2.5ns, CL = 50pF, RL - See Figure 4

CHARACTERISTICS		SYMBOL	VCC (V)	AMBIENT TEMPERATURE (TA) 0°C to +70°C MIN	MAX	-55°C to +125°C MIN	MAX	UNITS
Propagation Delays: An ⟷ Bn	FCT543	tPLH, tPHL	5†	3	8.5	3	10	ns
	FCT544	tPLH, tPHL	5	3	10.5	3	12	ns
$\overline{LEBA}$ to An or $\overline{LEAB}$ to Bn	FCT543	tPLH, tPHL	5	3	12.5	3	14	ns
	FCT544	tPLH, tPHL	5	3	14.5	3	17	ns
$\overline{CEBA}$ or $\overline{CEAB}$ to An or Bn		tPLZ, tPHZ	5	2.5	9	2.5	13	ns
$\overline{OEBA}$ or $\overline{OEAB}$ to An or Bn		tPZL, tPZH	5	2.5	12	2.5	14	ns
Power Dissipation Capacitance		CPD§	-					pF
Min. (Valley) VOHV During Switching of Other Outputs (Output Under Test Not Switching)		VOHV See Figure 1	5	0.5 Typical @ +25°C				V
Max. (Peak) VOLP During Switching of Other Outputs (Output Under Test Not Switching)		VOLP See Figure 1	5	1 Typical @ +25°C				V
Input Capacitance		CI	-	-	10	-	10	pF
3-State Output Capacitance		CO	-	-	15	-	15	pF

†5V: min. is @ 5.5V
max. is @ 4.5V
5V: min. is @ 5.25V for 0°C to +70°C
max. is @ 4.75V for 0°C to +70°C

§CPD, measured per function, is used to determine the dynamic power consumption.
PD (per package) = VCC ICC + Σ (VCC^2 fi CPD + VO^2 fo CL + VCC ΔICC D) where:
VCC = supply voltage
ΔICC = flow through current x unit load
CL = output load capacitance
D = duty cycle of input high
fo = output frequency
fi = input frequency

PARAMETER MEASUREMENT INFORMATION



NOTES:
1. VOLP is measured with respect to a ground reference near the output under test. VOHV is measured with respect to VOH.
2. Input pulses have the following characteristics: PRR ≤ 1MHz, tr = 2.5ns, tf = 2.5ns, skew 1ns.
3. R.F. fixture with 700-MHz design rules required. IC should be soldered into test board and bypassed with 0.1μF capacitor. Scope and probes require 700-MHz bandwidth.

Figure 1 - Simultaneous switching transient waveforms.

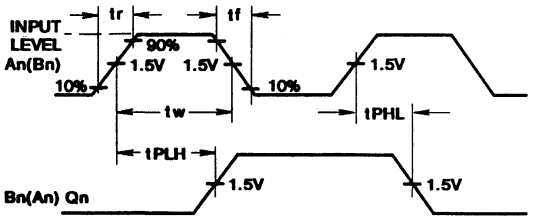


Figure 2 - CD54/74FCT543 propagation delay times.

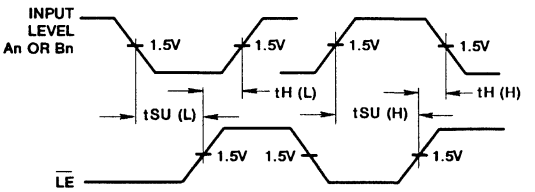
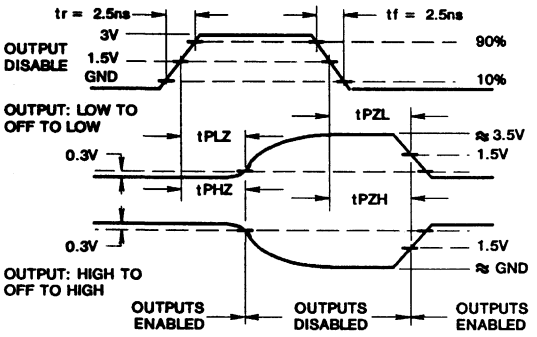
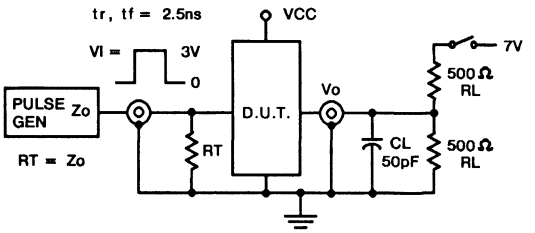


Figure 3 - CD54/74FCT543 setup and hold times.

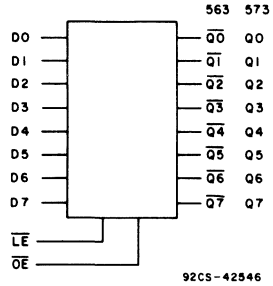




TEST	SWITCH POSITION
tPLZ, tPZL, OPEN DRAIN	CLOSED
tPHZ, tPZH, tPLH, tPHL	OPEN

Figure 4 - Three-state propagation delay times and test circuit.

CD54/74FCT563, CD54/74FCT573



FUNCTIONAL DIAGRAM

Octal Transparent Latch, 3-State

CD54/74FCT563 - Inverting
CD54/74FCT573 - Non-Inverting

Type Features:
- *Buffered inputs*
- *Typical propagation delay: 3.5 ns @ V_{CC} = 5 V, T_A = 25°C, C_L = 50 pF*

3

The CD54/74FCT563 and CD54/74FCT573 octal transparent latches use a small-geometry BiMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output-HIGH level to two diode drops below V_{CC}. This resultant lowering of output swing (0 to 3.7V) reduces power bus ringing (a source of EMI) and minimizes V_{CC} bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 32 to 48 milliamperes.

The CD54/74FCT563 and CD54/74FCT573 outputs are transparent to the inputs when the Latch Enable ($\overline{LE}$) is HIGH. When the Latch Enable ($\overline{LE}$) goes LOW, the data is latched. The Output Enable ($\overline{OE}$) controls the 3-state outputs. When the Output Enable ($\overline{OE}$) is HIGH, the outputs are in the high-impedance state. The latch operation is independent of the state of the Output Enable.

The CD54/74FCT563 and CD54/74FCT573 are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over two temperature ranges: Commercial (0 to 70°C) and Extended Industrial (-55 to +125°C).

The CD54FCT563 and CD54FCT573 are also available in chip form (H suffix). These unpackaged devices are operable over the -55 to +125°C temperature range.

Family Features:
- *SCR-latchup-resistant CMOS process and circuit design*
- *Speed of bipolar FAST*/AS/S with significantly reduced power consumption*
- *48/32-mA output sink current (commercial/extended industrial)*
- *Output voltage swing limited to 3.7 V @ V_{CC} = 5 V*
- *Controlled output-edge rates*
- *Input/output isolation to V_{CC}*
- *BiMOS technology with low quiescent power*

*FAST is a registered trademark of Fairchild Semiconductor Corp.

TRUTH TABLE

Output Enable	Latch Enable	Data	FCT563 Output	FCT573 Output
L	H	H	L	H
L	H	L	H	L
L	L	l	H	L
L	L	h	L	H
H	X	X	Z	Z

L = Low voltage level
H = High voltage level
l = Low voltage level one setup time prior to the high-to-low latch enable transition.
h = High voltage level one setup time prior to the high-to-low latch enable transition.
X = Don't care
Z = High-impedance state

Printed in USA/6-89

File Number **2304**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (V_{CC}) ..... -0.5 to 6 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ V) ..... -20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ V) ..... -50 mA
DC OUTPUT SINK CURRENT PER Output Pin, I_O ..... +70 mA
DC OUTPUT SOURCE CURRENT per Output Pin, I_O ..... -30 mA
DC V_{CC} CURRENT (I_{CC}) ..... 140 mA
DC GROUND CURRENT (I_{GND}) ..... 400 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE E, M ..... -55 to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only ..... +300°C

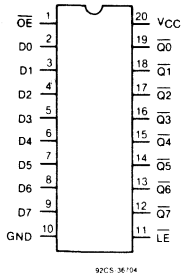
RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

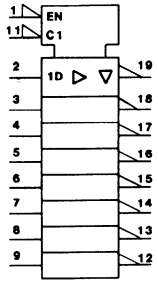
CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V_{CC}*:			
CD74 Series, T_A = 0 to 70°C	4.75	5.25	V
CD54 Series, T_A = -55 to +125°C	4.5	5.5	V
DC Input Voltage, V_I	0	V_{CC}	
DC Output Voltage, V_O	0	$\leq V_{CC}$	
Operating Temperature, T_A	-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv	0	10	ns/V

*Unless otherwise specified, all voltages are referenced to ground.

CD54/74FCT563

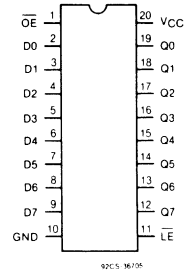


TERMINAL ASSIGNMENT

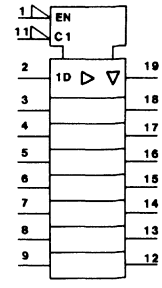


IEC LOGIC SYMBOL

CD54/74FCT573



TERMINAL ASSIGNMENT



IEC LOGIC SYMBOL

STATIC ELECTRICAL CHARACTERISTICS
FCT Series:
74FCT Commercial Temperature Range, 0 to 70°C; V_{CC} max = 5.25 V, V_{CC} min = 4.75 V
54FCT Extended Industrial Temperature Range, -55 to +125°C; V_{CC} max = 5.5 V, V_{CC} min = 4.5 V

CHARACTERISTIC		TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
					+25		0 to +70		-55 to +125		
		V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage	V_{IL}			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage	V_{OH}	V_{IH} or V_{IL}	-15	MIN.	2.4	—	2.4	—	—	—	V
			-12		2.4	—	—	—	2.4	—	
Low-Level Output Voltage	V_{OL}	V_{IH} or V_{IL}	48	MIN.	—	0.55	—	0.55	—	—	
			32		—	0.55	—	—	—	0.55	
High-Level Input Current	I_{IH}	V_{CC}		MAX.	—	0.1	—	1	—	1	μA
Low-Level Input Current	I_{IL}	GND		MAX.	—	-0.1	—	-1	—	-1	μA
3-State Leakage Current	I_{OZH}	V_{CC}		MAX.	—	0.5	—	10	—	10	μA
	I_{OZL}	GND		MAX.	—	-0.5	—	-10	—	-10	
Short-Circuit Output Current*	I_{OS}	V_{CC} or GND V_O = 0		MAX.	-60	—	-60	—	-60	—	mA
Input Clamp Voltage	V_{IK}	V_{CC} or GND	-18	MIN.	—	-1.2	—	-1.2	—	-1.2	V
Quiescent Supply Current, MSI	I_{CC}	V_{CC} or GND	0	MAX.	—	8	—	80	—	500	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load	ΔI_{CC}	3.4 V†		MAX.	—	1.6	—	1.6	—	2	mA

*Not more than one output should be shorted at one time. Test duration should not exceed 100 ms.
†Inputs that are not measured are at V_{CC} or Gnd.

FCT Input Loading: All inputs are 1 unit load. Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 1.6 mA max. @ 70°C.

3

PREREQUISITE FOR SWITCHING:

CHARACTERISTIC	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			0 to +70		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
$\overline{LE}$ Pulse Width	t_W	5†	6	—	6	—	ns
Setup Time, Data to $\overline{LE}$	t_{SU}	5	2	—	2	—	
Hold Time, Data to $\overline{LE}$	t_H	5	1.5	—	1.5	—	

†5 V min. is @ 4.5 V
5 V min. is @ 4.75 V for 0 to +70° C

SWITCHING CHARACTERISTICS: t_r, t_f = 2.5 ns, C_L = 50 pF, R_L—See Fig. 4

CHARACTERISTIC		SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) — °C				UNITS
				0 to +70		-55 to +125		
				MIN.	MAX.	MIN.	MAX.	
Propagation Delays:								
Data to Outputs	573	t_{PLH}	5†	1.5	8	1.5	8.5	ns
	563	t_{PHL}		1.5	8	1.5	8.5	
$\overline{LE}$ to Outputs	573	t_{PLH}	5	2	13	2	15	
	563	t_{PHL}		1.5	13	1.5	14	
Output Enable Times	573	t_{PZL}	—	1.5	12	1.5	13.5	
	563	t_{PZH}	—	1.5	11	1.5	12.5	
Output Disable Times	573	t_{PLZ}	—	1.5	7.5	1.5	10	
	563	t_{PHZ}	—	1.5	7	1.5	8.5	
Power Dissipation Capacitance	573	C_{PD}§	—					pF
	563							
Min. (Valley) V_{OHV} During Switching of Other Outputs (Output Under Test Not Switching)		V_{OHV} See Fig. 1	5	0.5 Typ. @ 25° C				V
Max. (Peak) V_{OLP} During Switching of Other Outputs (Output Under Test Not Switching)		V_{OLP} See Fig. 1	5	1 Typ. @ 25° C				
Input Capacitance		C_I	—	—	10	—	10	pF
3-State Output Capacitance		C_O	—	—	15	—	15	

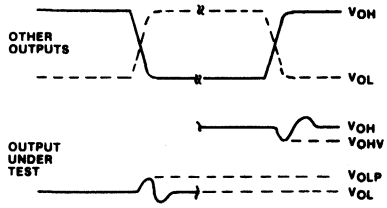
†5 V: min. is @ 5.5 V
max. is @ 4.5 V
5V: min. is @ 5.25 V for 0 to +70° C
max. is @ 4.75 V for 0 to +70° C

§C_{PD}, measured per latch, is used to determine the dynamic power consumption.

P_D (per package) = $V_{CC}\, I_{CC} + \Sigma\,(V_{CC}^2\, f_i\, C_{PD} + V_o^2\, f_o\, C_L + V_{CC}\, \Delta\, I_{CC} D)$ where V_{CC} = supply voltage

ΔI_{CC} = flow-through current x unit load
C_L = output load capacitance
D = duty cycle of input high
f_o = output frequency
f_i = input frequency

PARAMETER MEASUREMENT INFORMATION



NOTES:
1. V_{OLP} IS MEASURED WITH RESPECT TO A GROUND REFERENCE NEAR THE OUTPUT UNDER TEST. V_{OHV} IS MEASURED WITH RESPECT TO V_{OH}.
2. INPUT PULSES HAVE THE FOLLOWING CHARACTERISTICS: PRR ≤ 1 MHz, t_r = 3 ns, t_f = 3 ns, SKEW 1 ns.
3. R.F. FIXTURE WITH 700-MHz DESIGN RULES REQUIRED. IC SHOULD BE SOLDERED INTO TEST BOARD AND BYPASSED WITH 0.1 μF CAPACITOR. SCOPE AND PROBES REQUIRE 700-MHz BANDWIDTH.

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Fig. 1 - Simultaneous switching transient waveforms.

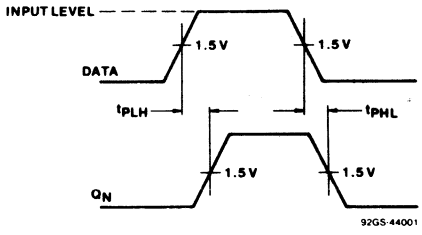


Fig. 2 - Data to Qn output propagation delays.

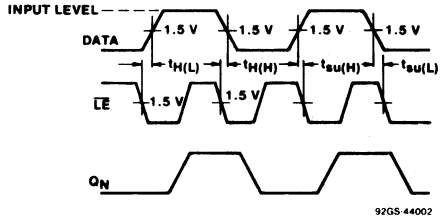
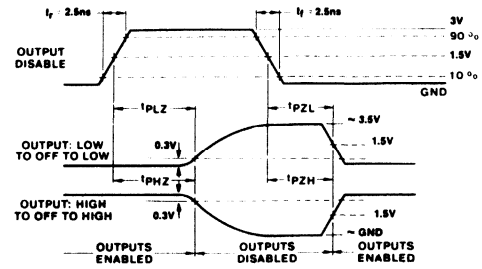
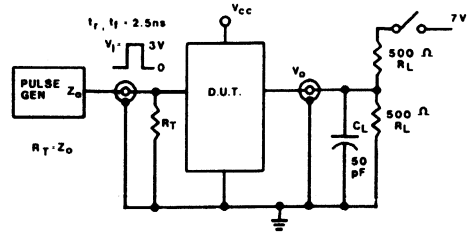


Fig. 3 - Latch Enable prerequisite times.





TEST	SWITCH POSITION
t_{PLZ} t_{PZL} OPEN DRAIN	CLOSED
t_{PHZ} t_{PZH} t_{PLH} t_{PHL}	OPEN

92CM-43518

Fig. 4 - Three-state propagation delay times and test circuit.

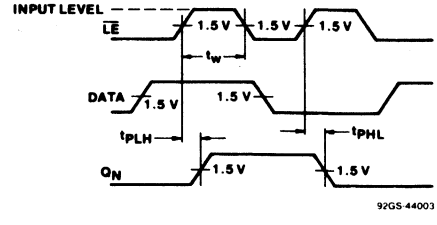
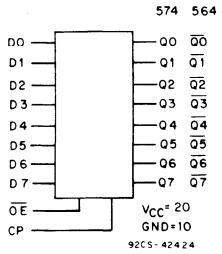


Fig. 5 - Latch Enable propagation delays.

CD54/74FCT564, CD54/74FCT574



FUNCTIONAL DIAGRAM

Octal D-Type Flip-Flop, 3-State

Positive-Edge-Triggered

CD54/74FCT564 - Inverting
CD54/74FCT574 - Non-Inverting

Type Features:
- *Buffered inputs*
- *Typical propagation delay: 3.5 ns @ V_{CC} = 5 V, T_A = 25° C, C_L = 50 pF*

The CD54/74FCT564 and CD54/74FCT574 octal D-type, 3-state, positive-edge-triggered flip-flops use a small-geometry BiMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output-HIGH level to two diode drops below V_{CC}. This resultant lowering of output swing (0 to 3.7 V) reduces power bus ringing (a source of EMI) and minimizes V_{CC} bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 32 to 48 milliamperes.

The eight flip-flops enter data into their registers on the LOW-to-HIGH transition of the clock (CP). The Output Enable ($\overline{OE}$) controls the 3-state outputs and is independent of the register operation. When the Output Enable ($\overline{OE}$) is HIGH, the outputs are in the high-impedance state. The CD54/74FCT564 and CD54/74FCT574 share the same configurations; the CD54/74FCT564, however, has inverted outputs and the CD54/74FCT574 has non-inverted outputs.

The CD54/74FCT564 and CD54/74FCT574 are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over two temperature ranges: Commercial (0 to 70° C) and Extended Industrial (-55 to +125° C).

The CD54FCT564 and CD54FCT574 are also available in chip form (H suffix). These unpackaged devices are operable over the -55 to +125° C temperature range.

Family Features:
- *SCR-latchup-resistant CMOS process and circuit design*
- *Speed of bipolar FAST*/AS/S with significantly reduced power consumption*
- *48/32-mA output sink current (commercial/extended industrial)*
- *Output voltage swing limited to 3.7 V @ V_{CC} = 5 V*
- *Controlled output-edge rates*
- *Input/output isolation to V_{CC}*
- *BiMOS technology with low quiescent power*

*FAST is a registered trademark of Fairchild Semiconductor Corp.

TRUTH TABLE

INPUTS			OUTPUTS	
			564	574
$\overline{OE}$	CP	Dn	$\overline{Qn}$	Qn
L	⎍	H	L	H
L	⎍	L	H	L
L	L	X	$\overline{Q0}$	Q0
H	X	X	Z	Z

H = High level (steady state)
L = Low level (steady state)
X = Don't care
⎍ = Transition from low to high level.
Q0 = The level of Q before the indicated steady-state input conditions were established.
$\overline{Q0}$ = The level of $\overline{Q}$ before the indicated steady-state input conditions were established.
Z = High impedance

Printed in USA/6-89

File Number **2295**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}) ..... -0.5 to 6 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ V) ..... -20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ V) ..... -50 mA
DC OUTPUT SINK CURRENT per Output Pin, I_O ..... +70 mA
DC OUTPUT SOURCE CURRENT per Output Pin, I_O ..... -30 mA
DC V_{CC} CURRENT (I_{CC}) ..... 140 mA
DC GROUND CURRENT (I_{GND}) ..... 400 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100° C (PACKAGE TYPE E) ..... 500 mW
For T_A = +100 to +125° C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/° C to 300 mW
For T_A = -55 to +70° C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125° C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/° C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE E, M ..... -55 to +125° C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265° C
Unit inserted into PC board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only ..... +300° C

3

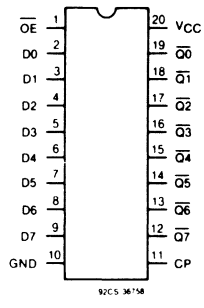
RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

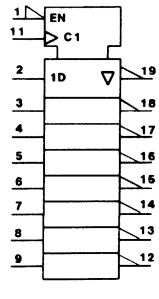
CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V_{CC}*:			
CD74 Series, T_A = 0 to 70° C	4.75	5.25	V
CD54 Series, T_A = -55 to +125° C	4.5	5.5	V
DC Input Voltage, V_I	0	V_{CC}	
DC Output Voltage, V_O	0	≤ V_{CC}	
Operating Temperature, T_A	-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv	0	10	ns/V

*Unless otherwise specified, all voltages are referenced to ground.

CD54/74FCT564

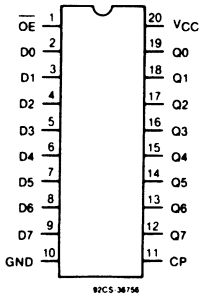


TERMINAL ASSIGNMENT



IEC LOGIC SYMBOL

CD54/74FCT574



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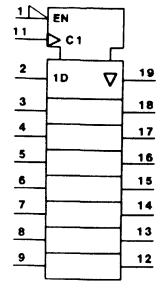


IEC LOGIC SYMBOL

STATIC ELECTRICAL CHARACTERISTICS
FCT Series:

74FCT Commercial Temperature Range, 0 to 70°C; V_{CC} max = 5.25 V, V_{CC} min = 4.75 V

54FCT Extended Industrial Temperature Range, -55 to +125°C; V_{CC} max = 5.5 V, V_{CC} min = 4.5 V

CHARACTERISTICS		TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
					+25		0 to +70		-55 to +125		
		V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage	V_{IL}			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage	V_{OH}	V_{IH} or V_{IL}	-15	MIN.	2.4	—	2.4	—	—	—	V
			-12		2.4	—	—	—	2.4	—	
Low-Level Output Voltage	V_{OL}	V_{IH} or V_{IL}	48	MIN.	—	0.55	—	0.55	—	—	
			32		—	0.55	—	—	—	0.55	
High-Level Input Current	I_{IH}	V_{CC}		MAX.	—	0.1	—	1	—	1	μA
Low-Level Input Current	I_{IL}	GND		MAX.	—	-0.1	—	-1	—	-1	μA
3-State Leakage Current	I_{OZH}	V_{CC}		MAX.	—	0.5	—	10	—	10	μA
	I_{OZL}	GND		MAX.	—	-0.5	—	-10	—	-10	
Short-Circuit Output Current*	I_{OS}	V_{CC} or GND V_O = 0		MAX.	-60	—	-60	—	-60	—	mA
Input Clamp Voltage	V_{IK}	V_{CC} or GND	-18	MIN.	—	-1.2	—	-1.2	—	-1.2	V
Quiescent Supply Current, MSI	I_{CC}	V_{CC} or GND	0	MAX.	—	8	—	80	—	500	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load	ΔI_{CC}	3.4 V†		MAX.	—	1.6	—	1.6	—	2	mA

*Not more than one output should be shorted at one time. Test duration should not exceed 100 ms.
†Inputs that are not measured are at V_{CC} or Gnd.

FCT Input Loading: All inputs are 1 unit load. Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 1.6 mA max. @ 70°C.

PREREQUISITE FOR SWITCHING

CHARACTERISTIC		SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) — °C				UNITS
				0 to +70		-55 to +125		
				MIN.	MAX.	MIN.	MAX.	
Clock Pulse Width	574	t_w	5†	7	—	7	—	ns
	564			7	—	7.5	—	
Setup Time Data to Clock		t_{SU}	5	2	—	2.5	—	
Hold Time Data to Clock	574	t_H	5	2	—	2	—	
	564			2	—	2.5	—	
Maximum Clock Frequency		f_{MAX}	5	70	—	60	—	MHz

†5 V: min. is @ 4.5 V
5 V: min. is @ 4.75 V for 0 to +70°C

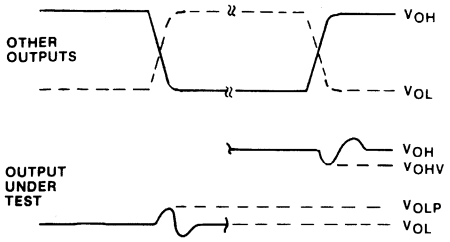
SWITCHING CHARACTERISTICS: t_r, t_f = 2.5 ns, C_L = 50 pF, R_L — See Fig. 4

CHARACTERISTIC	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) — °C				UNITS
			0 to +70		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Clock to Q 574	t_{PLH} t_{PHL}	5†	2	10	2	11	ns
Clock to $\overline{Q}$ 564	t_{PLH} t_{PHL}	5	1.5	10	1.5	11	
Output Enable and Disable to Q 574	t_{PLZ} t_{PHZ}	5	1.5	8	1.5	8	
	t_{PZL} t_{PZH}	5	1.5	12.5	1.5	14	
Output Enable and Disable to $\overline{Q}$ 564	t_{PLZ} t_{PHZ}	5	1.5	8	1.5	8	
	t_{PZL} t_{PZH}	5	1.5	12.5	1.5	14	
Power Dissipation Capacitance	C_{PD}§	—					pF
Min. (Valley) V_{OHV} During switching of other outputs (Output under test not switching)	V_{OHV} See Fig. 1	5	0.5 Typ. @ 25°C				V
Max. (Peak) V_{OLP} During switching of other outputs (Output under test not switching)	V_{OLP} See Fig. 1	5	1 Typ. @ 25°C				
Input Capacitance	C_I	—	—	10	—	10	pF
3-State Output Capacitance	C_O	—	—	15	—	15	

†5V: min. is @ 5.5 V
max. is @ 4.5 V
5V: min. is @ 5.25 V for 0 to +70°C
max. is @ 4.75 V for 0 to +70°C

§C_{PD}, measured per flip-flop, is used to determine the dynamic power consumption.
P_D (per package) = $V_{CC} I_{CC} + \Sigma (V_{CC}^2 f_i C_{PD} + V_o^2 f_o C_L + V_{CC} \Delta I_{CC} D)$ where V_{CC} = supply voltage
ΔI_{CC} = flow-through current x unit load
C_L = output load capacitance
D = duty cycle of input high
f_o = output frequency
f_i = input frequency

PARAMETER MEASUREMENT INFORMATION



NOTES:
1. V_{OLP} IS MEASURED WITH RESPECT TO A GROUND REFERENCE NEAR THE OUTPUT UNDER TEST. V_{OHV} IS MEASURED WITH RESPECT TO V_{OH}.
2. INPUT PULSES HAVE THE FOLLOWING CHARACTERISTICS: PRR ≤ 1 MHz, t_r = 3 ns, t_f = 3 ns, SKEW 1 ns.
3. R.F. FIXTURE WITH 700-MHz DESIGN RULES REQUIRED. IC SHOULD BE SOLDERED INTO TEST BOARD AND BYPASSED WITH 0.1 μF CAPACITOR. SCOPE AND PROBES REQUIRE 700-MHz BANDWIDTH.

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Fig. 1 - Simultaneous switching transient waveforms.

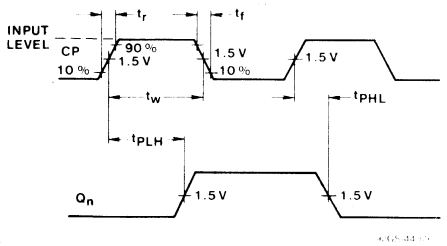


Fig. 2 - Propagation delay times.

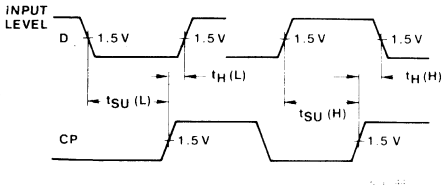
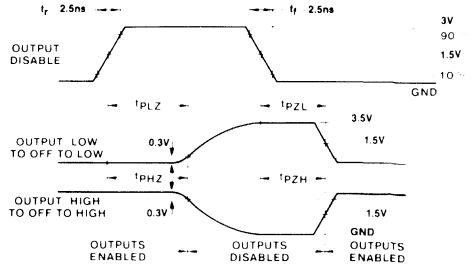
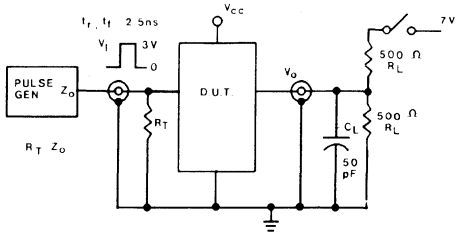


Fig. 3 - Setup and hold times.





TEST	SWITCH POSITION
t_{PLZ} t_{PZL} OPEN DRAIN	CLOSED
t_{PHZ} t_{PZH} t_{PLH} t_{PHL}	OPEN

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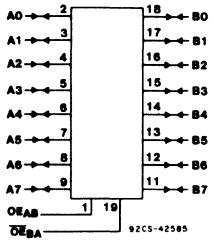
Fig. 4 - Three-state propagation delay times and test circuit.

CD54/74FCT623



FUNCTIONAL DIAGRAM

Octal-Bus Transceiver, 3-State, Non-Inverting

Type Features:
- *Buffered inputs*
- *Typical propagation delay: 3 ns @ V_{CC} = 5 V, T_A = 25°C, C_L = 50 pF*

3

The CD54/74FCT623 octal-bus transceivers use a small-geometry BiMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output-HIGH level to two diode drops below V_{CC}. This resultant lowering of output swing (0 to 3.7 V) reduces power bus ringing (a source of EMI) and minimizes V_{CC} bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 48 to 64 milliamperes.

The CD54/74FCT623 are non-inverting, 3-state, bidirectional transceiver-buffers that allow for two-way transmission from "A" bus to "B" bus or "B" bus to "A" bus, depending on the logic levels of the Output Enable (OE_{AB}, $\overline{OE}_{BA}$) inputs.

The dual Output Enable provision gives these devices the capability to store data by simultaneously enabling OE_{AB} and $\overline{OE}_{BA}$. Each output reinforces its input under these conditions, and when all other data sources to the bus lines are at high impedance, both sets of bus lines will remain in their last states.

The CD54/74FCT623 are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over two temperature ranges: Commercial (0 to 70°C) and Extended Industrial (-55 to +125°C).

The CD54FCT623 is also available in chip form (H suffix). This unpackaged device is operable over the -55 to +125°C temperature range.

Family Features:
- *SCR-latchup-resistant CMOS process and circuit design*
- *Speed of bipolar FAST*/AS/S with significantly reduced power consumption*
- *64/48-mA output sink current (commercial/extended industrial)*
- *Output voltage swing limited to 3.7 V @ V_{CC} = 5 V*
- *Controlled output-edge rates*
- *Input/output isolation to V_{CC}*
- *BiMOS technology with low quiescent power*

*FAST is a Registered Trademark of Fairchild Semiconductor Corp.

TRUTH TABLE

OUTPUT ENABLE INPUTS		OPERATION
$\overline{OE}_{BA}$	OE_{AB}	
L	L	B DATA TO A BUS
H	H	A DATA TO B BUS
H	L	ISOLATION
L	H	B DATA TO A BUS, A DATA TO B BUS

H = High level, L = Low level

Note: To prevent excess currents in the High-Z (isolation) modes, all I/O terminals should be terminated with 10 kΩ to 1 MΩ resistors.

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File Number 2302

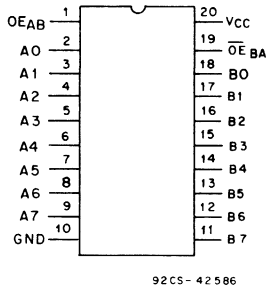
MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE (V_{CC}) ..... -0.5 to 6 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ V) ..... -20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ V) ..... -50 mA
DC OUTPUT SINK CURRENT per Output Pin, I_O ..... +70 mA
DC OUTPUT SOURCE CURRENT per Output Pin, I_O ..... -30 mA
DC V_{CC} CURRENT (I_{CC}) ..... 140 mA
DC GROUND CURRENT (I_{GND}) ..... 528 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE E, M ..... -55 to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only ..... +300°C

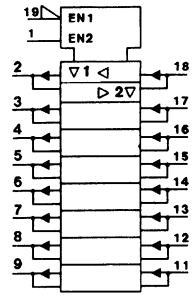
RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V_{CC}*:			
CD74 Series, T_A = 0 to 70°C	4.75	5.25	V
CD54 Series, T_A = -55 to +125°C	4.5	5.5	V
DC Input Voltage, V_I	0	V_{CC}	V
DC Output Voltage, V_O	0	$\leq V_{CC}$	V
Operating Temperature, T_A	-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv	0	10	ns/V

*Unless otherwise specified, all voltages are referenced to ground.



TERMINAL ASSIGNMENT



IEC LOGIC SYMBOL

STATIC ELECTRICAL CHARACTERISTICS
FCT Series:

74FCT Commercial Temperature Range, 0 to 70°C; V_{CC} max = 5.25 V, V_{CC} min = 4.75 V
54FCT Extended Industrial Temperature Range, -55 to +125°C; V_{CC} max = 5.5 V, V_{CC} min = 4.5 V

CHARACTERISTICS		TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
					+25		0 to +70		-55 to +125		
		V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage	V_{IL}			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage	V_{OH}	V_{IH} or V_{IL}	-15	MIN.	2.4	—	2.4	—	—	—	V
			-12		2.4	—	—	—	2.4	—	
Low-Level Output Voltage	V_{OL}	V_{IH} or V_{IL}	64	MIN.	—	0.55	—	0.55	—	—	
			48		—	0.55	—	—	—	0.55	
High-Level Input Current	I_{IH}	V_{CC}		MAX.	—	0.1	—	1	—	1	μA
Low-Level Input Current	I_{IL}	GND		MAX.	—	-0.1	—	-1	—	-1	μA
3-State Leakage Current	I_{OZH}	V_{CC}		MAX.	—	0.5	—	10	—	10	μA
	I_{OZL}	GND		MAX.	—	-0.5	—	-10	—	-10	
Short-Circuit Output Current*	I_{OS}	V_{CC} or GND V_O = 0		MAX.	-60	—	-60	—	-60	—	mA
Input Clamp Voltage	V_{IK}	V_{CC} or GND	-18	MIN.	—	-1.2	—	-1.2	—	-1.2	V
Quiescent Supply Current, MSI	I_{CC}	V_{CC} or GND	0	MAX.	—	8	—	80	—	500	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load	ΔI_{CC}	3.4 V†		MAX.	—	1.6	—	1.6	—	2	mA

*Not more than one output should be shorted at one time. Test duration should not exceed 100 ms.
†Inputs that are not measured are at V_{CC} or Gnd.

FCT Input Loading: All inputs are 1 unit load. Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 1.6 mA max. @ 70°C.

3

SWITCHING CHARACTERISTICS: t_r, t_f = 2.5 ns, C_L = 50 pF, R_L - See Fig. 3

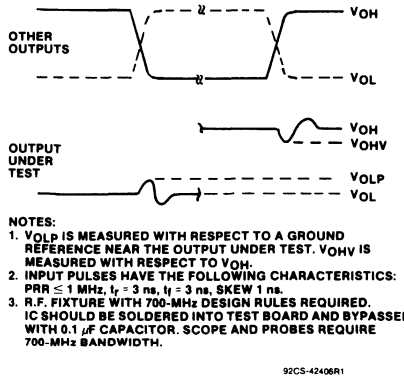
CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) -°C				UNITS
			0 to +70		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Data to Outputs	t_{PLH} t_{PHL}	5†	1.5	7	1.5	7.5	ns
Output Disable to Output	t_{PLZ} t_{PHZ}	5	1.5	7.5	1.5	10	ns
Output Enable to Output	t_{PZH} t_{PZL}	5	1.5	9.5	1.5	10	ns
Power Dissipation Capacitance	C_{PD}§	—					pF
Min. (Valley) V_{OHV} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OHV} See Fig. 1	5	0.5 Typ. @ 25°C				V
Max. (Peak) V_{OLP} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OLP} See Fig. 1	5	1 Typ. @ 25°C				V
Input Capacitance	C_I	—	—	10	—	10	pF
3-State Output Capacitance	C_O	—	—	15	—	15	pF

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

5 V: min. is @ 5.25 V for 0 to +70°C
max. is @ 4.75 V for 0 to +70°C

§C_{PD}, measured per function, is used to determine the dynamic power consumption.
P_D (per package) = $V_{CC}\ I_{cc} + \Sigma\ (V_{CC}^2\ f_i\ C_{PD} + V_O^2\ f_o\ C_L + V_{CC}\ \Delta I_{CC} D)$
where V_{cc} = supply voltage
ΔI_{CC} = flow-through current x unit load
C_L = output load capacitance
D = duty cycle of input high
f_o = output frequency
f_i = input frequency

PARAMETER MEASUREMENT INFORMATION



NOTES:
1. V_{OLP} IS MEASURED WITH RESPECT TO A GROUND REFERENCE NEAR THE OUTPUT UNDER TEST. V_{OHV} IS MEASURED WITH RESPECT TO V_{OH}.
2. INPUT PULSES HAVE THE FOLLOWING CHARACTERISTICS: PRR ≤ 1 MHz, t_r = 3 ns, t_f = 3 ns, SKEW 1 ns.
3. R.F. FIXTURE WITH 700-MHz DESIGN RULES REQUIRED. IC SHOULD BE SOLDERED INTO TEST BOARD AND BYPASSED WITH 0.1 μF CAPACITOR. SCOPE AND PROBES REQUIRE 700-MHz BANDWIDTH.

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Fig. 1 - Simultaneous switching transient waveforms.

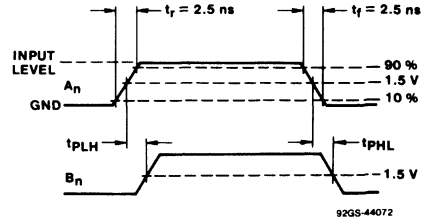
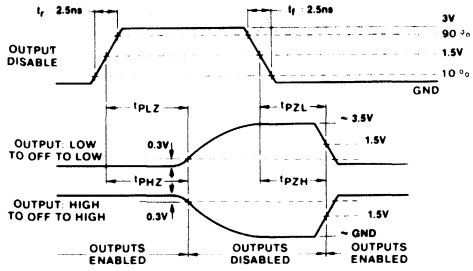
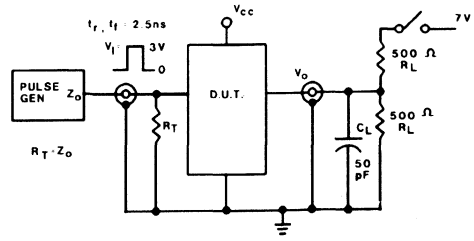


Fig. 2 - Propagation delay times.





TEST	SWITCH POSITION
t_{PLZ} t_{PZL} OPEN DRAIN	CLOSED
t_{PHZ} t_{PZH} t_{PLH} t_{PHL}	OPEN

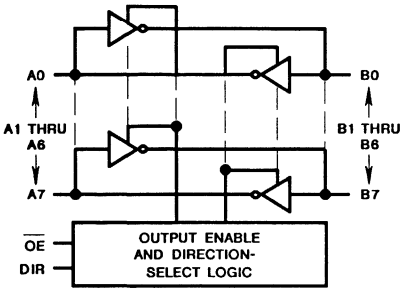
Fig. 3 - Three-state propagation delay times and test circuit.

3

CD54/74FCT640, CD54/74FCT643

Octal Bus Transceivers, 3-State

CD54/74FCT640 - Inverting
CD54/74FCT643 - True/Inverting



INVERTING FCT640 FUNCTIONAL DIAGRAM

Type Features:

- *Buffered inputs*
- *Typical propagation delay: 3ns @ VCC = 5V, TA = +25°C, CL = 50pF*

The CD54/74FCT640 and CD54/74FCT643 use a small-geometry BiMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output-HIGH level to two diode drops below VCC. This resultant lowering of output swing (0V to 3.7V) reduces power bus ringing (a source of EMI) and minimizes VCC bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 48 to 64 milliamperes.

These octal bus transceivers are designed for asynchronous two-way communication between data buses.

The CD54/74FCT640 is an octal inverting buffer; the CD54/74FCT643 is an octal true/inverting buffer.

The direction of data flow (A to B, B to A) is controlled by the DIR input.

Outputs are enabled by a low on the Output Enable input ($\overline{OE}$); a high $\overline{OE}$ puts these devices in the high-impedance mode.

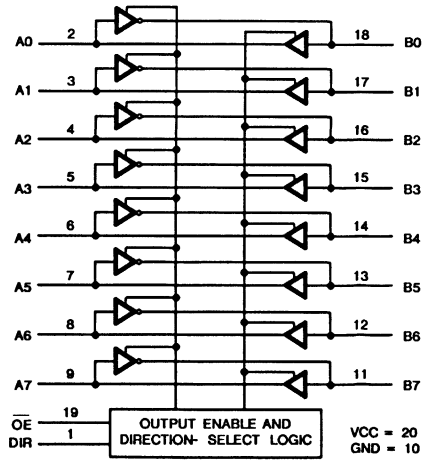
The CD54/74FCT640 and CD54/74FCT643 are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over two temperature ranges: Commercial (0°C to +70°C) and Extended Industrial (-55°C to +125°C).

The CD54FCT640 and CD54FCT643 are also available in chip form (H suffix). These unpackaged devices are operable over the -55°C to +125°C temperature range.

Family Features:

- *SCR-latchup-resistant CMOS process and circuit design*
- *Speed of bipolar FAST*/AS/S with significantly reduced power consumption*
- *64/48-mA output sink current (commercial/extended industrial)*
- *Output voltage swing limited to 3.7V @ VCC = 5V*
- *Controlled output-edge rates*
- *Input/output isolation to VCC*
- *BiMOS technology with low quiescent power*

* FAST is a registered trademark of Fairchild Semiconductor Corp.



TRUE/INVERTING FCT643 FUNCTIONAL DIAGRAM

Printed in USA/8-89

File Number **2398**

TRUTH TABLE

CONTROL INPUTS		FCT640 DATA PORT STATUS		FCT643 DATA PORT STATUS	
$\overline{OE}$	DIR	An	Bn	An	Bn
L	L	$\overline{O}$	I	O	I
H	H	Z	Z	Z	Z
H	L	Z	Z	Z	Z
L	H	I	$\overline{O}$	I	$\overline{O}$

To prevent excess currents in the High-Z modes, all I/O terminals should be terminated with 10kΩ to 1MΩ resistors.

H = HIGH
L = LOW
I = Input
O = Output (Same Level as Input)
$\overline{O}$ = Output (Inversion of Input Level)
Z = High Impedance

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (VCC) ..... -0.5V to 6V
DC INPUT DIODE CURRENT, IIK (for VI < -0.5V) ..... -20mA
DC OUTPUT DIODE CURRENT, IOK (for VO < -0.5V) ..... -50mA
DC OUTPUT SINK CURRENT per Output Pin, IO ..... +70mA
DC OUTPUT SOURCE CURRENT per Output Pin, IO ..... -30mA
DC VCC CURRENT (ICC) 140mA
DC GROUND CURRENT (IGND) 528mA
POWER DISSIPATION PER PACKAGE (PD)
For TA = -55°C to +100°C (PACKAGE TYPE E) 500mW
For TA = +100°C to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8mW/°C to 300mW
For TA = -55°C to +70°C (PACKAGE TYPE M) 400mW
For TA = +70°C to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6mW/°C to 70mW
OPERATING-TEMPERATURE RANGE (TA):
PACKAGE TYPE E, M ..... -55°C to +125°C
STORAGE TEMPERATURE (Tstg) ..... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 in. ± 1/32 in. (1.59mm ± 0.79mm) from case for 10s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59mm) with solder contacting lead tips only ..... +300°C

RECOMMENDED OPERATING CONDITIONS:

The following are normal operating ranges for these devices. For maximum reliability, devices should always be operated within these ranges.

CHARACTERISTIC		LIMITS MIN	LIMITS MAX	UNITS
Supply-Voltage Range, VCC*:	CD74 Series, TA = 0°C to 70°C	4.75	5.25	V
	CD54 Series, TA = -55°C to +125°C	4.5	5.5	V
DC Input Voltage, VI		0	VCC	V
DC Output Voltage, VO		0	≤ VCC	V
Operating Temperature, TA		-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv		0	10	ns/V

* Unless otherwise specified, all voltages are referenced to ground.

STATIC ELECTRICAL CHARACTERISTICS

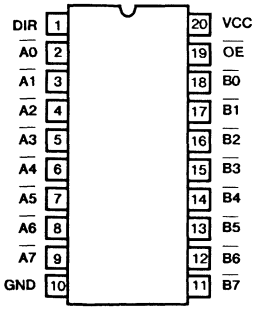
FCT Series: 74FCT Commercial Temperature Range, 0°C to +70°C; VCC max = 5.25V, VCC min = 4.75V
54FCT Extended Industrial Temperature Range, -55°C to +125°C; VCC max = 5.5V, VCC min = 4.5V

CHARACTERISTICS		TEST CONDITIONS VI (V)	TEST CONDITIONS IO (mA)	VCC (V)	AMBIENT TEMPERATURE (TA) +25°C MIN	+25°C MAX	0°C to +70°C MIN	0°C to +70°C MAX	-55°C to +125°C MIN	-55°C to +125°C MAX	UNITS
High-Level Input Voltage	VIH			4.5 to 5.5	2	-	2	-	2	-	V
Low-Level Input Voltage	VIL			4.5 to 5.5	-	0.8	-	0.8	-	0.8	V
High-Level Output Voltage	VOH	VIH or	-15	MIN	2.4	-	2.4	-	-	-	V
		VIL	-12	MIN	2.4	-	-	-	2.4	-	V
Low-Level Output Voltage	VOL	VIH or	64	MIN	-	0.55	-	0.55	-	-	V
		VIL	48	MIN	-	0.55	-	-	-	0.55	V
High-Level Input Current	IIH	VCC		MAX	-	0.1	-	1	-	1	µA
Low-Level Input Current	IIL	GND		MAX	-	-0.1	-	-1	-	-1	µA
3-State Leakage Current	IOZH	VCC		MAX	-	0.5	-	10	-	10	µA
	IOZL	GND		MAX	-	-0.5	-	-10	-	-10	µA
Short-Circuit Output Current *	IOS	VCC or GND VO = 0		MAX	-60	-	-60	-	-60	-	mA
Input Clamp Voltage	VIK	VCC or GND	-18	MIN	-	-1.2	-	-1.2	-	-1.2	V
Quiescent Supply Current, MSI	ICC	VCC or GND	0	MAX	-	8	-	80	-	500	µA
Additional Quiescent Supply Current per Input Pin TTL Inputs High, 1 Unit Load	ΔICC	3.4V†		MAX	-	1.6	-	1.6	-	2	mA

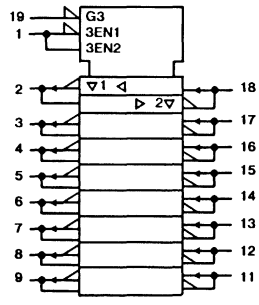
* Not more than one output should be shorted at one time. Test duration should not exceed 100ms.
† Inputs that are not measured are at VCC or GND.

FCT Input Loading: All inputs are 1 unit load. Unit load is ΔICC limit specified in Static Characteristics Chart, e.g., 1.6mA max. @ +70°C.

CD54/74FCT640 TYPES

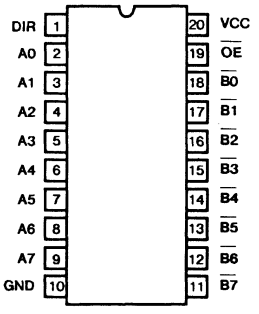


TERMINAL ASSIGNMENT



IEC LOGIC SYMBOL

CD54/74FCT643 TYPES



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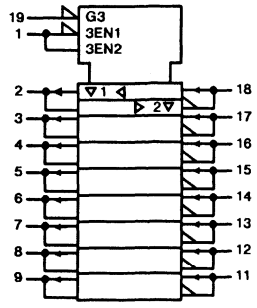


IEC LOGIC SYMBOL

SWITCHING CHARACTERISTICS

FCT Series: tr, tf = 2.5ns, CL = 50pF, RL - See Figure 3

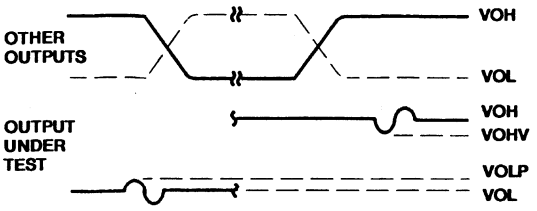
CHARACTERISTICS		SYMBOL	VCC (V)	AMBIENT TEMPERATURE (TA) 0°C to +70°C MIN	0°C to +70°C MAX	-55°C to +125°C MIN	-55°C to +125°C MAX	UNITS
Propagation Delays: Data to Outputs	FCT640 A→$\overline{B}$, FCT640 B→$\overline{A}$, FCT643 A→$\overline{B}$	tPLH, tPHL	5†	2	7	2	8	ns
	FCT643 B→A,	tPLH, tPHL	5†	2	6.5	2	7	ns
Output Disable to Output	FCT640	tPLZ, tPHZ	5	2	10	2	12	ns
	FCT643	tPLZ, tPHZ	5	2	10	2	12	ns
Output Enable to Output	FCT640	tPZL, tPZH	5	2	13	2	16	ns
	FCT643	tPZL, tPZH	5	2	13	2	16	ns
Power Dissipation Capacitance		CPD§	-					pF
Min. (Valley) VCHV During Switching of Other Outputs (Output Under Test Not Switching)		VCHV See Fig. 1	5	0.5 Typ. @ +25°C				V
Max. (Peak) VOLP During Switching of Other Outputs (Output Under Test Not Switching)		VOLP See Fig. 1	5	1 Typ. @ +25°C				V
Input Capacitance		CI	-	-	10	-	10	pF
3-State Output Capacitance		CO	-	-	15	-	15	pF

†5V: min. is @ 5.5V
max. is @ 4.5V
5V: min. is @ 5.25V for 0°C to +70°C
max. is @ 4.75V for 0°C to +70°C

§CPD, measured per function, is used to determine the dynamic power consumption.
PD (per package) = VCC ICC + Σ (VCC^2 fi CPD + VO^2 fo CL + VCC ΔICC D) where:
VCC = supply voltage
ΔICC = flow through current x unit load
CL = output load capacitance
D = duty cycle of input high
fo = output frequency
fi = input frequency

3

PARAMETER MEASUREMENT INFORMATION



NOTES:

1. VOLP is measured with respect to a ground reference near the output under test. VOHV is measured with respect to VOH.
2. Input pulses have the following characteristics: PRR ≤ 1MHz, tr = 2.5ns, tf = 2.5ns, skew 1ns.
3. R.F. fixture with 700-MHz design rules required. IC should be soldered into test board and bypassed with 0.1μF capacitor. Scope and probes require 700-MHz bandwidth.

Figure 1 - Simultaneous switching transient waveforms.

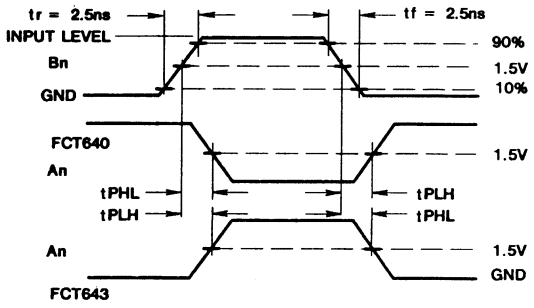
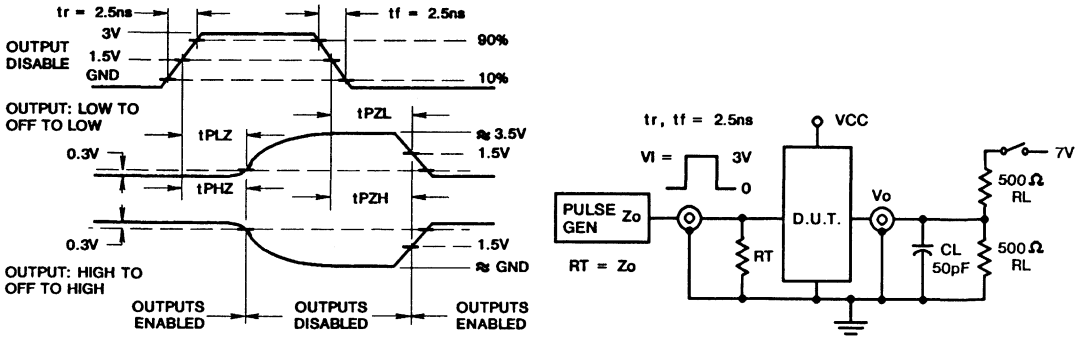


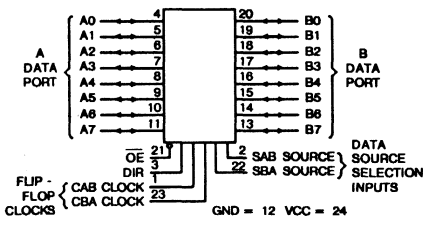
Figure 2 - Propagation delay times.



TEST	SWITCH POSITION
tPLZ, tPZL, OPEN DRAIN	CLOSED
tPHZ, tPZH, tPLH, tPHL	OPEN

Figure 3 - Three-state propagation delay times and test circuit.

CD54/74FCT646, CD54/74FCT648



FUNCTIONAL DIAGRAM

Octal Bus Transceivers/ Registers, 3-State

CD54/74FCT646 - Non-Inverting
CD54/74FCT648 - Inverting

Type Features:
- *Buffered inputs*
- *Typical propagation delay: 3ns @ VCC = 5V, TA = +25°C, CL = 50pF*

3

The CD54/74FCT646 and CD54/74FCT648 3-state, octal bus tranceivers/registers use a small-geometry BiMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output-HIGH level to two diode drops below VCC. This resultant lowering of output swing (0 to 3.7V) reduces power bus ringing (a source of EMI) and minimizes VCC bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 48 to 64 milliamperes.

These devices are bus transceivers with D-type flip-flops which act as internal storage registers on the LOW-to-HIGH transition of either CAB or CBA clock inputs. Output Enable ($\overline{OE}$) and Direction (DIR) inputs control the transceiver functions. Data present at the high-impedance output can be stored in either register or both but only one of the two buses can be enabled as outputs at any one time. The Select controls (SAB and SBA) can multiplex stored and transparent (real time) data. The Direction control determines which data bus will receive data when the Output Enable ($\overline{OE}$) is LOW. In the high-impedance mode (Output Enable HIGH), A data can be stored in one register and B data can be stored in the other register. The clocks are not gated with the Direction (DIR) and Output Enable ($\overline{OE}$) terminals; data at the A or B terminals can be clocked into the storage flip-flops at any time.

Family Features:
- *SCR-latchup-resistant CMOS process and circuit design*
- *Speed of bipolar FAST*/AS/S with significantly reduced power consumption*
- *64/48-mA output sink current (commercial/extended industrial)*
- *Output voltage swing limited to 3.7V @ VCC = 5V*
- *Controlled output-edge rates*
- *Input/output isolation to VCC*
- *BiMOS technology with low quiescent power*

* *FAST is a registered trademark of Fairchild Semiconductor Corp.*

The CD54/74FCT646 and CD54/74FCT648 are supplied in 24-lead dual-in-line narrow-body plastic packages (EN suffix) and in 24-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over two temperature ranges: Commercial (0 to +70°C) and Extended Industrial (-55°C to +125°C).

The CD54FCT646 and CD54FCT648 are also available in chip form (H suffix). These unpackaged device are operable over the -55°C to +125°C temperature range.

FUNCTION TABLE

INPUTS						DATA I/O#		OPERATION OR FUNCTION	
$\overline{OE}$	DIR	CAB	CBA	SAB	SBA	A0 THRU A7	B0 THRU B7	CD54/74FCT646	CD54/74FCT648
X	X	↓	X	X	X	Input	Not Specified	Store A, B unspecified	Store A, B unspecified
X	X	X	↓	X	X	Not Specified	Input	Store B, A unspecified	Store B, A unspecified
H	X	↓	↓	X	X	Input	Input	Store A and B Data	Store A and B Data
H	X	H or L	H or L	X	X			Isolation, hold storage	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus	Stored B Data to A Bus
L	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus	Real-Time A Data to B Bus
L	H	H or L	X	H	X			Stored A Data to B Bus	Stored A Data to B Bus

#The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition of the clock inputs. To prevent excess currents in the High-Z modes, all I/O terminals should be terminated with 10kΩ resistors.

Printed in USA/8-89

File Number **2393**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (VCC) ..... -0.5V to 6V
DC INPUT DIODE CURRENT, IIK (for VI < -0.5V) ..... -20mA
DC OUTPUT DIODE CURRENT, IOK (for VO < -0.5V) ..... -50mA
DC OUTPUT SINK CURRENT per Output Pin, IO ..... +70mA
DC OUTPUT SOURCE CURRENT per Output Pin, IO ..... -30mA
DC VCC CURRENT (ICC) 140mA
DC GROUND CURRENT (IGND) 528mA
POWER DISSIPATION PER PACKAGE (PD):
For TA = -55°C to +100°C (PACKAGE TYPE E) 500mW
For TA = +100°C to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8mW/°C to 300mW
For TA = -55°C to +70°C (PACKAGE TYPE M) 400mW
For TA = +70°C to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6mW/°C to 70mW
OPERATING-TEMPERATURE RANGE (TA):
PACKAGE TYPE E, M ..... -55°C to +125°C
STORAGE TEMPERATURE (Tstg) ..... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 in. ± 1/32 in. (1.59mm ± 0.79mm) from case for 10s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59mm) with solder contacting lead tips only ..... +300°C

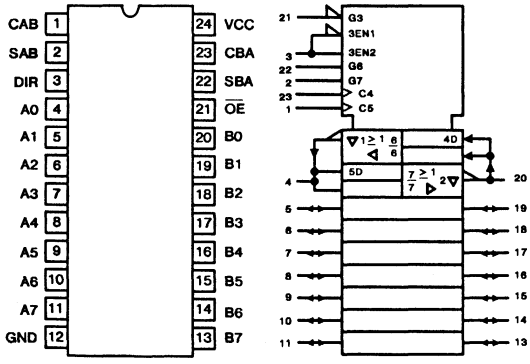
RECOMMENDED OPERATING CONDITIONS:

The following are normal operating ranges for these devices. For maximum reliability, devices should always be operated within these ranges.

CHARACTERISTIC		LIMITS MIN	LIMITS MAX	UNITS
Supply-Voltage Range, VCC*:	CD74 Series, TA = 0°C to 70°C	4.75	5.25	V
	CD54 Series, TA = -55°C to +125°C	4.5	5.5	V
DC Input Voltage, VI		0	VCC	V
DC Output Voltage, VO		0	≤ VCC	V
Operating Temperature, TA		-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv		0	10	ns/V

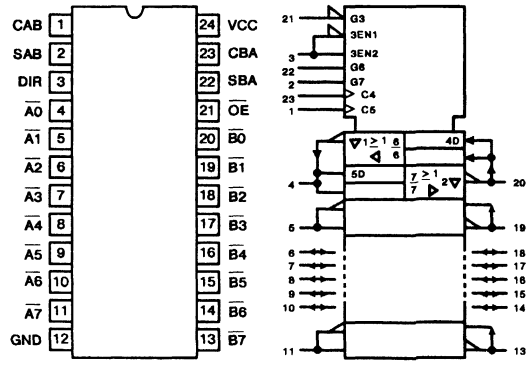
* Unless otherwise specified, all voltages are referenced to ground.

CD54/74FCT646 TYPES



TERMINAL ASSIGNMENT — IEC LOGIC SYMBOL

CD54/74FCT648 TYPES



TERMINAL ASSIGNMENT — IEC LOGIC SYMBOL

STATIC ELECTRICAL CHARACTERISTICS

FCT Series: 74FCT Commercial Temperature Range, 0°C to +70°C; VCC max = 5.25V, VCC min = 4.75V
54FCT Extended Industrial Temperature Range, -55°C to +125°C; VCC max = 5.5V, VCC min = 4.5V

CHARACTERISTICS		TEST CONDITIONS VI (V)	TEST CONDITIONS IO (mA)	VCC (V)	AMBIENT TEMPERATURE (TA) +25°C MIN	+25°C MAX	0°C to +70°C MIN	0°C to +70°C MAX	-55°C to +125°C MIN	-55°C to +125°C MAX	UNITS
High-Level Input Voltage	VIH			4.5 to 5.5	2	-	2	-	2	-	V
Low-Level Input Voltage	VIL			4.5 to 5.5	-	0.8	-	0.8	-	0.8	V
High-Level Output Voltage	VOH	VIH or	-15	MIN	2.4	-	2.4	-	-	-	V
		VIL	-12	MIN	2.4	-	-	-	2.4	-	V
Low-Level Output Voltage	VOL	VIH or	64	MIN	-	0.55	-	0.55	-	-	V
		VIL	48	MIN	-	0.55	-	-	-	0.55	V
High-Level Input Current	IIH	VCC		MAX	-	0.1	-	1	-	1	µA
Low-Level Input Current	IIL	GND		MAX	-	-0.1	-	-1	-	-1	µA
3-State Leakage Current	IOZH	VCC		MAX	-	0.5	-	10	-	10	µA
	IOZL	GND		MAX	-	-0.5	-	-10	-	-10	µA
Short-Circuit Output Current *	IOS	VCC or GND VO = 0		MAX	-60	-	-60	-	-60	-	mA
Input Clamp Voltage	VIK	VCC or GND	-18	MIN	-	-1.2	-	-1.2	-	-1.2	V
Quiescent Supply Current, MSI	ICC	VCC or GND	0	MAX	-	8	-	80	-	500	µA
Additional Quiescent Supply Current per Input Pin TTL Inputs High, 1 Unit Load	ΔICC	3.4V†		MAX	-	1.6	-	1.6	-	2	mA

* Not more than one output should be shorted at one time. Test duration should not exceed 100ms.
† Inputs that are not measured are at VCC or GND.

FCT Input Loading: All inputs are 1 unit load. Unit load is ΔICC limit specified in Static Characteristics Chart, e.g., 1.6mA max. @ +70°C.

3

PREREQUISITE FOR SWITCHING

CHARACTERISTICS	SYMBOL	VCC (V)	AMBIENT TEMPERATURE (TA) 0°C to +70°C MIN	0°C to +70°C MAX	-55°C to +125°C MIN	-55°C to +125°C MAX	UNITS
Maximum Frequency	fMAX	5†	85	-	85	-	MHz
Data to Clock Setup Time	tSU	5	4	-	4.5	-	ns
Data to Clock Hold Time	tH	5	2	-	2	-	ns
Clock Pulse Width	tW	5	6	-	6	-	ns

†5V: min. is @ 4.5V
5V: min. is @ 4.75V for 0°C to +70°C

SWITCHING CHARACTERISTICS

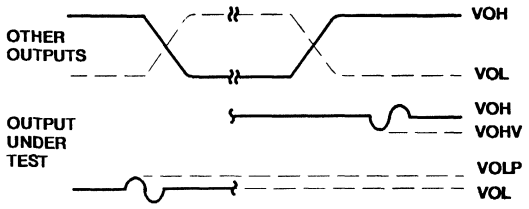
FCT Series: tr, tf = 2.5ns, CL = 50pF, RL - See Figure 4

CHARACTERISTICS		SYMBOL	VCC (V)	AMBIENT TEMPERATURE (TA) 0°C to +70°C MIN	0°C to +70°C MAX	-55°C to +125°C MIN	-55°C to +125°C MAX	UNITS
Propagation Delays: Store A Data to B Bus, Store B Data to A Bus	FCT646	tPLH, tPHL	5†	2	9	2	10	ns
Store $\overline{A}$ Data to B Bus, Store $\overline{B}$ Data to A Bus	FCT648	tPLH, tPHL	5	2	9	2	10	ns
A Data to B Bus, B Data to A Bus	FCT646	tPLH, tPHL	5	2	9	2	11	ns
$\overline{A}$ Data to B Bus, $\overline{B}$ Data to A Bus	FCT648	tPLH, tPHL	5	2	8	2	9	ns
Select to Data	FCT646	tPLH, tPHL	5	2	11	2	12	ns
	FCT648	tPLH, tPHL	5	2	11	2	12	ns
3-State Enabling Time, Bus to Output or Register to Output	FCT646	tPZL, tPZH	5	2	14	2	15	ns
	FCT648	tPZL, tPZH	5	2	15	2	18	ns
3-State Disabling Time, Bus to Output or Register to Output	FCT646	tPLZ, tPHZ	5	2	9	2	11	ns
	FCT648	tPLZ, tPHZ	5	2	9	2	11	ns
Power Dissipation Capacitance		CPD§	-					pF
Min. (Valley) VOHV During Switching of Other Outputs (Output Under Test Not Switching)		VOHV See Figure 1	5	0.5 Typical @ +25°C				V
Max. (Peak) VOLP During Switching of Other Outputs (Output Under Test Not Switching)		VOLP See Figure 1	5	1 Typical @ +25°C				V
Input Capacitance		CI	-	-	10	-	10	pF
3-State Output Capacitance		CO	-	-	15	-	15	pF

†5V: min. is @ 5.5V
max. is @ 4.5V
5V: min. is @ 5.25V for 0°C to +70°C
max. is @ 4.75V for 0°C to +70°C

§CPD, measured per latch, is used to determine the dynamic power consumption.
PD (per package) = VCC ICC + Σ (VCC^2 fi CPD + VO^2 fo CL + VCC ΔICC D) where:
VCC = supply voltage
ΔICC = flow through current x unit load
CL = output load capacitance
D = duty cycle of input high
fo = output frequency
fi = input frequency

PARAMETER MEASUREMENT INFORMATION



NOTES:

1. VOLP is measured with respect to a ground reference near the output under test. VOHV is measured with respect to VOH.
2. Input pulses have the following characteristics: PRR ≤ 1MHz, tr = 2.5ns, tf = 2.5ns, skew 1ns.
3. R.F. fixture with 700-MHz design rules required. IC should be soldered into test board and bypassed with 0.1µF capacitor. Scope and probes require 700-MHz bandwidth.

Figure 1 - Simultaneous switching transient waveforms.

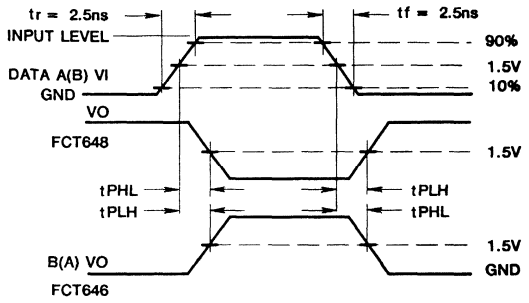


Figure 2 - propagation delay times.

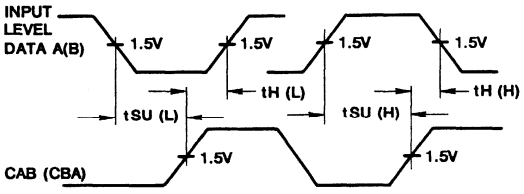
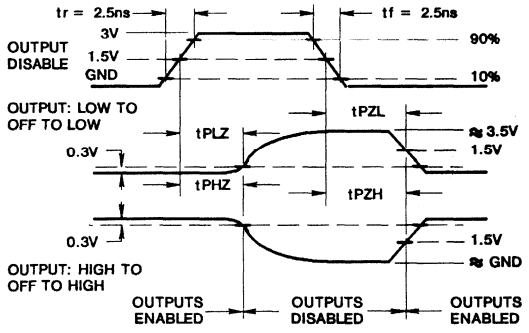
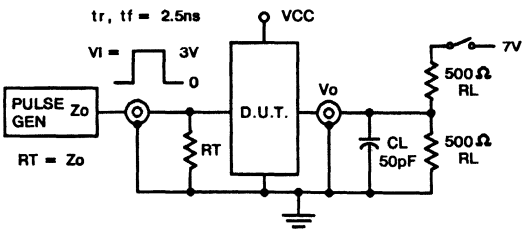


Figure 3 - setup and hold times.

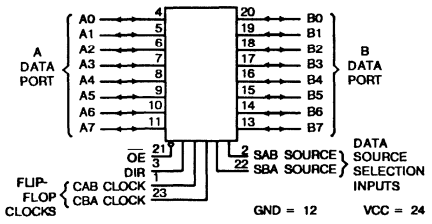




TEST	SWITCH POSITION
tPLZ, tPZL, OPEN DRAIN	CLOSED
tPHZ, tPZH, tPLH, tPHL	OPEN

Figure 4 - Three-state propagation delay times and test circuit.

CD54/74FCT647, CD54/74FCT649



FUNCTIONAL DIAGRAM

Octal Bus Transceivers/Registers, with Open Drain

CD54/74FCT647 - Non-Inverting
CD54/74FCT649 - Inverting

Type Features:
- *Buffered inputs*
- *Typical propagation delay: 3.5ns @ VCC = 5V, TA = +25°C, CL = 50pF*

The CD54/74FCT647 and CD54/74FCT649 open-drain, octal-bus tranceivers/registers use a small-geometry BiMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output-HIGH level to two diode drops below VCC. This resultant lowering of output swing (0 to 3.7V) reduces power bus ringing (a source of EMI) and minimizes VCC bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 48 to 64 milliamperes.

These devices are bus transceivers with D-type flip-flops which act as internal storage registers on the LOW-to-HIGH transition of either CAB or CBA clock inputs. Output Enable ($\overline{OE}$) and Direction (DIR) inputs control the transceiver functions. Data present at the high-impedance output can be stored in either register or both but only one of the two buses can be enabled as outputs at any one time. The Select controls (SAB and SBA) can multiplex stored and transparent (real time) data. The Direction control determines which data bus will receive data when the Output Enable ($\overline{OE}$) is LOW. In the high-impedance mode (Output Enable HIGH), A data can be stored in one register and B data can be stored in the other register. The clocks are not gated with the Direction (DIR) and Output Enable ($\overline{OE}$) terminals; data at the A or B terminals can be clocked into the storage flip-flops at any time.

Family Features:
- *SCR-latchup-resistant CMOS process and circuit design*
- *Speed of bipolar FAST*/AS/S with significantly reduced power consumption*
- *64/48-mA output sink current (commercial/extended industrial)*
- *Output voltage swing limited to 3.7V @ VCC = 5V*
- *Controlled output-edge rates*
- *Input/output isolation to VCC*
- *BiMOS technology with low quiescent power*

** FAST is a registered trademark of Fairchild Semiconductor Corp.*

The CD54/74FCT647 and CD54/74FCT649 are supplied in 24-lead dual-in-line narrow-body plastic packages (EN suffix) and in 24-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over two temperature ranges: Commercial (0 to +70°C) and Extended Industrial (-55°C to +125°C).

The CD54FCT647 and CD54FCT649 are also available in chip form (H suffix). These unpackaged device are operable over the -55°C to +125°C temperature range.

FUNCTION TABLE

INPUTS						DATA I/O#		OPERATION OR FUNCTION	
$\overline{OE}$	DIR	CAB	CBA	SAB	SBA	A0 THRU A7	B0 THRU B7	CD54/74FCT647	CD54/74FCT649
X	X	↓	X	X	X	Input	Not Specified	Store A, B unspecified	Store A, B unspecified
X	X	X	↓	X	X	Not Specified	Input	Store B, A unspecified	Store B, A unspecified
H	X	↓	↓	X	X	Input	Input	Store A and B Data	Store A and B Data
H	X	H or L	H or L	X	X			Isolation, hold storage	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus	Real-Time $\overline{B}$ Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus	Stored $\overline{B}$ Data to A Bus
L	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus	Real-Time $\overline{A}$ Data to B Bus
L	H	H or L	X	H	X			Stored A Data to B Bus	Stored $\overline{A}$ Data to B Bus

#The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition of the clock inputs. To prevent excess currents in the High-Z modes, all I/O terminals should be terminated with 10kΩ resistors.

Printed in USA/8-89

File Number **2402**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (VCC) ..... -0.5V to 6V
DC INPUT DIODE CURRENT, IIK (for VI < -0.5V) ..... -20mA
DC OUTPUT DIODE CURRENT, IOK (for VO < -0.5V) ..... -50mA
DC OUTPUT SINK CURRENT per Output Pin, IO ..... +70mA
DC OUTPUT SOURCE CURRENT per Output Pin, IO ..... -30mA
DC VCC CURRENT (ICC) 140mA
DC GROUND CURRENT (IGND) 528mA
POWER DISSIPATION PER PACKAGE (PD):
For TA = -55°C to +100°C (PACKAGE TYPE E) 500mW
For TA = +100°C to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8mW/°C to 300mW
For TA = -55°C to +70°C (PACKAGE TYPE M) 400mW
For TA = +70°C to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6mW/°C to 70mW
OPERATING-TEMPERATURE RANGE (TA):
PACKAGE TYPE E, M ..... -55°C to +125°C
STORAGE TEMPERATURE (Tstg) ..... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 in. ± 1/32 in. (1.59mm ± 0.79mm) from case for 10s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59mm) with solder contacting lead tips only ..... +300°C

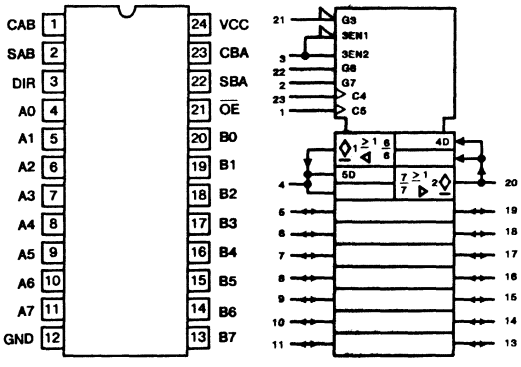
RECOMMENDED OPERATING CONDITIONS:

The following are normal operating ranges for these devices. For maximum reliability, devices should always be operated within these ranges.

CHARACTERISTIC		LIMITS MIN	LIMITS MAX	UNITS
Supply-Voltage Range, VCC*:	CD74 Series, TA = 0°C to 70°C	4.75	5.25	V
	CD54 Series, TA = -55°C to +125°C	4.5	5.5	V
DC Input Voltage, VI		40	VCC	V
DC Output Voltage, VO		0	≤ VCC	V
Operating Temperature, TA		-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv		0	10	ns/V

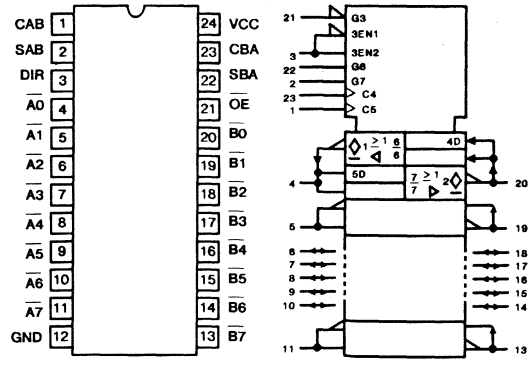
* Unless otherwise specified, all voltages are referenced to ground.

CD54/74FCT647 TYPES



TERMINAL ASSIGNMENT — IEC LOGIC SYMBOL

CD54/74FCT649 TYPES



TERMINAL ASSIGNMENT — IEC LOGIC SYMBOL

STATIC ELECTRICAL CHARACTERISTICS

FCT Series: 74FCT Commercial Temperature Range, 0°C to +70°C; VCC max = 5.25V, VCC min = 4.75V
54FCT Extended Industrial Temperature Range, -55°C to +125°C; VCC max = 5.5V, VCC min = 4.5V

CHARACTERISTICS		TEST CONDITIONS VI (V)	TEST CONDITIONS IO (mA)	VCC (V)	AMBIENT TEMPERATURE (TA) +25°C MIN	+25°C MAX	0°C to +70°C MIN	0°C to +70°C MAX	-55°C to +125°C MIN	-55°C to +125°C MAX	UNITS
High-Level Input Voltage	VIH			4.5 to 5.5	2	-	2	-	2	-	V
Low-Level Input Voltage	VIL			4.5 to 5.5	-	0.8	-	0.8	-	0.8	V
High-Level Output Voltage	VOH	VIH or	-15	MIN	2.4	-	2.4	-	-	-	V
		VIL	-12	MIN	2.4	-	-	-	2.4	-	V
Low-Level Output Voltage	VOL	VIH or	64	MIN	-	0.55	-	0.55	-	-	V
		VIL	48	MIN	-	0.55	-	-	-	0.55	V
High-Level Input Current	IIH	VCC		MAX	-	0.1	-	1	-	1	µA
Low-Level Input Current	IIL	GND		MAX	-	-0.1	-	-1	-	-1	µA
3-State Leakage Current	IOZH	VCC		MAX	-	0.5	-	10	-	10	µA
	IOZL	GND		MAX	-	-0.5	-	-10	-	-10	µA
Short-Circuit Output Current *	IOS	VCC or GND VO = 0		MAX	-60	-	-60	-	-60	-	mA
Input Clamp Voltage	VIK	VCC or GND	-18	MIN	-	-1.2	-	-1.2	-	-1.2	V
Quiescent Supply Current, MSI	ICC	VCC or GND	0	MAX	-	8	-	80	-	500	µA
Additional Quiescent Supply Current per Input Pin TTL Inputs High, 1 Unit Load	ΔICC	3.4V†		MAX	-	1.6	-	1.6	-	2	mA

* Not more than one output should be shorted at one time. Test duration should not exceed 100ms.
† Inputs that are not measured are at VCC or GND.

FCT Input Loading: All inputs are 1 unit load. Unit load is ΔICC limit specified in Static Characteristics Chart, e.g., 1.6mA max. @ +70°C.

PREREQUISITE FOR SWITCHING

CHARACTERISTICS	SYMBOL	VCC (V)	AMBIENT TEMPERATURE (TA) 0°C to +70°C MIN	0°C to +70°C MAX	-55°C to +125°C MIN	-55°C to +125°C MAX	UNITS
Data to Clock Setup Time	tSU	5	4	-	4.5	-	ns
Data to Clock Hold Time	tH	5	2	-	2	-	ns
Clock Pulse Width	tW	5	6	-	6	-	ns

†5V: min. is @ 4.5V
5V: min. is @ 4.75V for 0°C to +70°C

SWITCHING CHARACTERISTICS

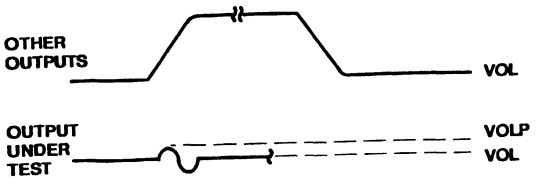
FCT Series: tr, tf = 2.5ns, CL = 50pF, RL - See Figure 3

CHARACTERISTICS		SYMBOL	VCC (V)	AMBIENT TEMPERATURE (TA) 0°C to +70°C MIN	0°C to +70°C MAX	-55°C to +125°C MIN	-55°C to +125°C MAX	UNITS
Propagation Delays: Stored A Data to B Bus, Stored B Data to A Bus	FCT647	tPZL	5†	2	9	2	10	ns
		tPLZ	5	2	9	2	11	ns
Stored $\overline{A}$ Data to B Bus, Stored $\overline{B}$ Data to A Bus	FCT649	tPZL	5	2	9	2	10	ns
		tPLZ	5	2	9	2	11	ns
A Data to B Bus, B Data to A Bus	FCT647	tPZL	5	2	9	2	11	ns
		tPLZ	5	2	9	2	11	ns
$\overline{A}$ Data to B Bus, $\overline{B}$ Data to A Bus	FCT649	tPZL	5	2	8	2	9	ns
		tPLZ	5	2	9	2	11	ns
Select to Data	FCT647, FCT649	tPZL	5	2	11	2	12	ns
		tPLZ	5	2	9	2	11	ns
Enabling Times, Bus to Output or Register to Output	FCT647	tPZL	5	2	14	2	15	ns
	FCT649	tPZL	5	2	15	2	18	ns
Disabling Times, Bus to Output or Register to Output	FCT647, FCT649	tPLZ	5	2	9	2	11	ns
Power Dissipation Capacitance		CPD§	-					pF
Max. (Peak) VOL During Switching of Other Outputs (Output Under Test Not Switching)		VOLP See Figure 1	5	1 Typical @ +25°C				V
Input Capacitance		CI	-	-	10	-	10	pF
Off-State Output Capacitance		CO	-	-	15	-	15	pF

†5V: min. is @ 5.5V
max. is @ 4.5V
5V: min. is @ 5.25V for 0°C to +70°C
max. is @ 4.75V for 0°C to +70°C

§CPD, measured per latch, is used to determine the dynamic power consumption.
PD (per package) = VCC ICC + Σ (VCC^2 fi CPD + VO^2 fo CL + VCC ΔICC D) where:
VCC = supply voltage
ΔICC = flow through current x unit load
CL = output load capacitance
D = duty cycle of input high
fo = output frequency
fi = input frequency

PARAMETER MEASUREMENT INFORMATION



NOTES:

1. VOLP is measured with respect to a ground reference near the output under test.
2. Input pulses have the following characteristics: PRR ≤ 1MHz, tr = 2.5ns, tf = 2.5ns, skew 1ns.
3. R.F. fixture with 700-MHz design rules required. IC should be soldered into test board and bypassed with 0.1μF capacitor. Scope and probes require 700-MHz bandwidth.

Figure 1 - Simultaneous switching transient waveforms.

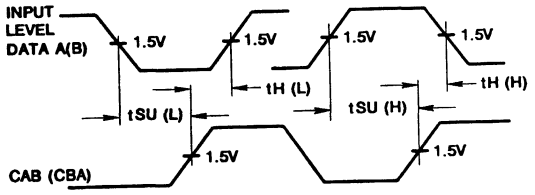


Figure 2 - Data setup and hold times.

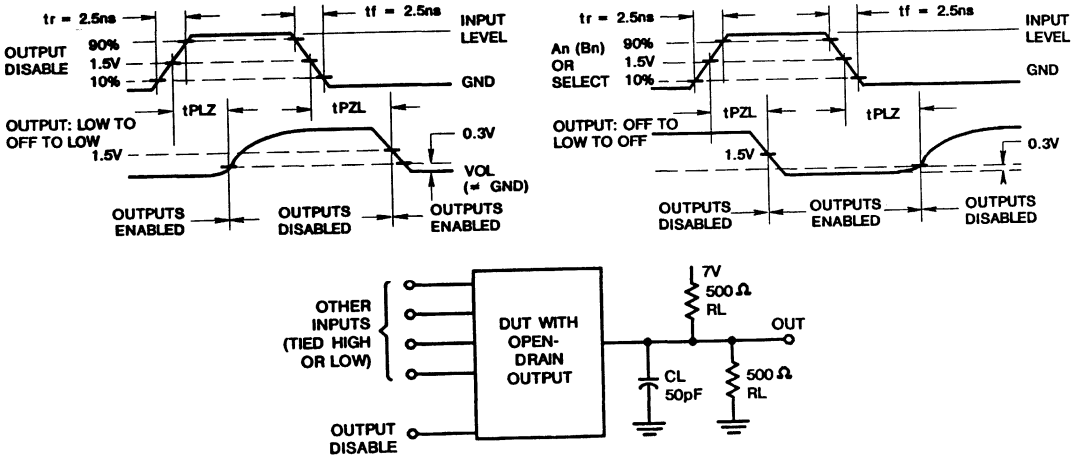
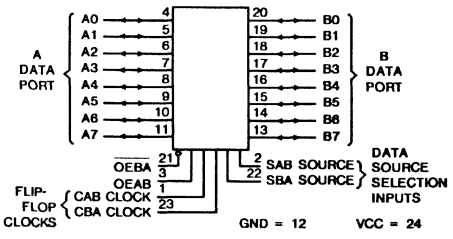


Figure 3 - Open-drain propagation delay times and test circuit.

CD54/74FCT651, CD54/74FCT652



CD54/74FCT652 FUNCTIONAL DIAGRAM

Octal Bus Transceivers/ Registers, 3-State

CD54/74FCT651 - Inverting
CD54/74FCT652 - Non-Inverting

Type Features:

- *Buffered inputs*
- *Typical propagation delay: 3ns @ VCC = 5V, TA = 25°C, CL = 50pF*

3

The CD54/74FCT651 and CD54/74FCT652 3-state, octal bus transceivers/registers use a small-geometry BiMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output-HIGH level to two diode drops below VCC. This resultant lowering of output swing (0V to 3.7V) reduces power bus ringing (a source of EMI) and minimizes VCC bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enchances switching speed and is capable of sinking 48 to 64 milliamperes.

These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Output Enables OEAB and $\overline{OEBA}$ are provided to control the transceiver functions. SAB and SBA control pins are provided to select whether real-time or stored data is transferred. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A LOW input level selects real-time data, and a HIGH selects stored data. The following examples demonstrate the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers.

Data on the A or B data bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CAB or CBA) regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and $\overline{OEBA}$. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

Family Features:

- *SCR-latchup-resistant CMOS process and circuit design*
- *Speed of bipolar FAST*/AS/S with significantly reduced power consumption*
- *64/48-mA output sink current (commercial/extended industrial)*
- *Output voltage swing limited to 3.7V @ VCC = 5V*
- *Controlled output-edge rates*
- *Input/output isolation to VCC*
- *BiMOS technology with low quiescent power*

* FAST is a registered trademark of Fairchild Semiconductor Corp.

The CD54/74FCT651 and CD54/74FCT652 are supplied in 24-lead dual-in-line narrow-body plastic packages (EN suffix) and in 24-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over two temperature ranges: Commercial (0°C to +70°C) and Extended Industrial (-55°C to +125°C).

The CD54FCT651 and CD54FCT652 are also available in chip form (H suffix). These unpackaged devices are operable over the -55°C to +125°C temperature range.

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File Number **2394**

FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION	
OEAB	$\overline{OEBA}$	CAB	CBA	SAB	SBA	A0 THRU A7	B0 THRU B7	CD54/74FCT651	CD54/74FCT652
L	H	H or L	H or L	X	X	Input	Input	Isolation *	Isolation *
L	H	⎍	⎍	X	X	Input	Input	Store A and B Data	Store A and B Data
X	H	⎍	H or L	X	X	Input	Unspecified †	Store A, Hold B	Store A, Hold B
H	H	⎍	⎍	X‡	X	Input	Output	Store A in both registers	Store A in both registers
L	X	H or L	⎍	X	X	Unspecified †	Input	Hold A, Store B	Hold, A Store B
L	L	⎍	⎍	X	X‡	Output	Input	Stored B in both registers	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-Time $\overline{B}$ Data to A Bus	Real-Time B Data to A Bus
L	L	X	H or L	X	H	Output	Input	Stored $\overline{B}$ Data to A Bus	Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time $\overline{A}$ Data to B Bus	Real-Time A Data to B Bus
H	H	H or L	X	H	X	Input	Output	Stored $\overline{A}$ Data to B Bus	Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored $\overline{A}$ Data to B Bus Stored $\overline{B}$ Data to A Bus	Stored A Data to B Bus Stored B Data to A Bus

* To prevent excess currents in the High-Z (isolation) modes, all I/O terminals should be terminated with 10kΩ to 1MΩ resistors.

† The data output functions may be enabled or disabled by various signals at the OEAB or $\overline{OEBA}$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

‡ Select control = L: clocks can occur simultaneously.
Select control = H: clocks must be staggered in order to load both registers.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (VCC) ..... -0.5V to 6V
DC INPUT DIODE CURRENT, IIK (for VI < -0.5V) ..... -20mA
DC OUTPUT DIODE CURRENT, IOK (for VO < -0.5V) ..... -50mA
DC OUTPUT SINK CURRENT per Output Pin, IO ..... +70mA
DC OUTPUT SOURCE CURRENT per Output Pin, IO ..... -30mA
DC VCC CURRENT (ICC) 140mA
DC GROUND CURRENT (IGND) 528mA
POWER DISSIPATION PER PACKAGE (PD):
For TA = -55°C to +100°C (PACKAGE TYPE E) 500mW
For TA = +100°C to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8mW/°C to 300mW
For TA = -55°C to +70°C (PACKAGE TYPE M) 400mW
For TA = +70°C to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6mW/°C to 70mW
OPERATING-TEMPERATURE RANGE (TA):
PACKAGE TYPE E, M ..... -55°C to +125°C
STORAGE TEMPERATURE (Tstg) ..... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 in. ± 1/32 in. (1.59mm ± 0.79mm) from case for 10s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59mm) with solder contacting lead tips only ..... +300°C

RECOMMENDED OPERATING CONDITIONS:

The following are normal operating ranges for these devices. For maximum reliability, devices should always be operated within these ranges.

CHARACTERISTIC		LIMITS MIN	LIMITS MAX	UNITS
Supply-Voltage Range, VCC*:	CD74 Series, TA = 0°C to 70°C	4.75	5.25	V
	CD54 Series, TA = -55°C to +125°C	4.5	5.5	V
DC Input Voltage, VI		0	VCC	V
DC Output Voltage, VO		0	≤ VCC	V
Operating Temperature, TA		-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv		0	10	ns/V

* Unless otherwise specified, all voltages are referenced to ground.

STATIC ELECTRICAL CHARACTERISTICS

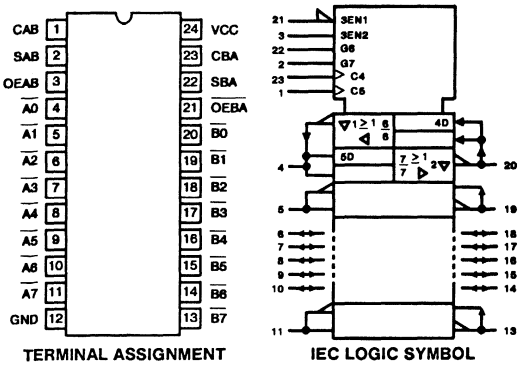
FCT Series: 74FCT Commercial Temperature Range, 0°C to +70°C; VCC max = 5.25V, VCC min = 4.75V
54FCT Extended Industrial Temperature Range, -55°C to +125°C; VCC max = 5.5V, VCC min = 4.5V

CHARACTERISTICS		TEST CONDITIONS VI (V)	TEST CONDITIONS IO (mA)	VCC (V)	AMBIENT TEMPERATURE (TA) +25°C MIN	+25°C MAX	0°C to +70°C MIN	0°C to +70°C MAX	-55°C to +125°C MIN	-55°C to +125°C MAX	UNITS
High-Level Input Voltage	VIH			4.5 to 5.5	2	-	2	-	2	-	V
Low-Level Input Voltage	VIL			4.5 to 5.5	-	0.8	-	0.8	-	0.8	V
High-Level Output Voltage	VOH	VIH or	-15	MIN	2.4	-	2.4	-	-	-	V
		VIL	-12	MIN	2.4	-	-	-	2.4	-	V
Low-Level Output Voltage	VOL	VIH or	64	MIN	-	0.55	-	0.55	-	-	V
		VIL	48	MIN	-	0.55	-	-	-	0.55	V
High-Level Input Current	IIH	VCC		MAX	-	0.1	-	1	-	1	µA
Low-Level Input Current	IIL	GND		MAX	-	-0.1	-	-1	-	-1	µA
3-State Leakage Current	IOZH	VCC		MAX	-	0.5	-	10	-	10	µA
	IOZL	GND		MAX	-	-0.5	-	-10	-	-10	µA
Short-Circuit Output Current *	IOS	VCC or GND VO = 0		MAX	-60	-	-60	-	-60	-	mA
Input Clamp Voltage	VIK	VCC or GND	-18	MIN	-	-1.2	-	-1.2	-	-1.2	V
Quiescent Supply Current, MSI	ICC	VCC or GND	0	MAX	-	8	-	80	-	500	µA
Additional Quiescent Supply Current per Input Pin TTL Inputs High, 1 Unit Load	ΔICC	3.4V†		MAX	-	1.6	-	1.6	-	2	mA

* Not more than one output should be shorted at one time. Test duration should not exceed 100ms.
† Inputs that are not measured are at VCC or GND.

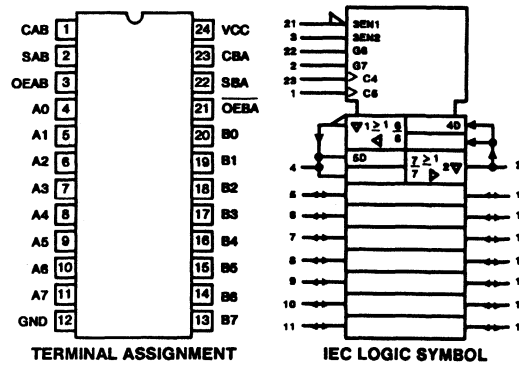
FCT Input Loading: All inputs are 1 unit load. Unit load is ΔICC limit specified in Static Characteristics Chart, e.g., 1.6mA max. @ +70°C.

CD54/74FCT651 TYPES



TERMINAL ASSIGNMENT — IEC LOGIC SYMBOL

CD54/74FCT652 TYPES



TERMINAL ASSIGNMENT — IEC LOGIC SYMBOL

PREREQUISITE FOR SWITCHING

CHARACTERISTICS	SYMBOL	VCC (V)	AMBIENT TEMPERATURE (TA)				UNITS
			0°C to +70°C		-55°C to +125°C		
			MIN	MAX	MIN	MAX	
Maximum Frequency	fMAX	5†	85	-	85	-	MHz
Data to Clock Setup Time	tSU	5	4	-	4.5	-	ns
Data to Clock Hold Time	tH	5	2	-	2	-	ns
Clock Pulse Width	tW	5	6	-	6	-	ns

†5V: min. is @ 4.5V
5V: min. is @ 4.75V for 0°C to +70°C

SWITCHING CHARACTERISTICS

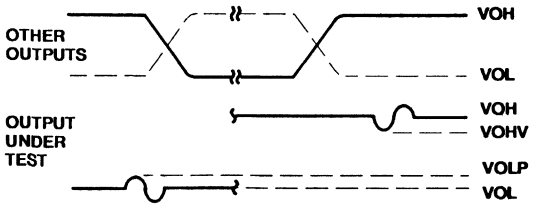
FCT Series: tr, tf = 2.5ns, CL = 50pF, RL - See Figure 4

CHARACTERISTICS		SYMBOL	VCC (V)	AMBIENT TEMPERATURE (TA)				UNITS
				0°C to +70°C		-55°C to +125°C		
				MIN	MAX	MIN	MAX	
Propagation Delays: Store A Data to B Bus Store B Data to A Bus	FCT652	tPLH, tPHL	5†	2	9	2	10	ns
Store $\overline{A}$ Data to B Bus Store $\overline{B}$ Data to A Bus	FCT651	tPLH, tPHL	5	2	9	2	10	ns
A Data to B Bus B Data to A Bus	FCT652	tPLH, tPHL	5	2	9	2	11	ns
$\overline{A}$ Data to B Bus $\overline{B}$ Data to A Bus	FCT651	tPLH, tPHL	5	2	8	2	9	ns
Select to Data	FCT651, FCT652	tPLH, tPHL	5	2	11	2	12	ns
3-State Enabling Time Bus to Output or Register to Output	FCT651	tPZL, tPZH	5	2	14	2	15	ns
	FCT652	tPZL, tPZH	5	2	15	2	18	ns
3-State Disabling Time Bus to Output or Register to Output	FCT651	tPLZ, tPHZ	5	2	9	2	11	ns
	FCT652	tPLZ, tPHZ	5	2	9	2	11	ns
Power Dissipation Capacitance		CPD§	-					pF
Min. (Valley) VOHV During Switching of Other Outputs (Output Under Test Not Switching)		VOHV See Figure 1	5	0.5 Typical @ +25°C				V
Max. (Peak) VOLP During Switching of Other Outputs (Output Under Test Not Switching)		VOLP See Figure 1	5	1 Typical @ +25°C				V
Input Capacitance		CI	-	-	10	-	10	pF
3-State Output Capacitance		CO	-	-	15	-	15	pF

†5V: min. is @ 5.5V
max. is @ 4.5V
5V: min. is @ 5.25V for 0°C to +70°C
max. is @ 4.75V for 0°C to +70°C

§CPD, measured per flip-flop, is used to determine the dynamic power consumption.
PD (per package) = VCC ICC + Σ (VCC^2 fi CPD + VO^2 fo CL + VCC ΔICC D) where:
VCC = supply voltage
ΔICC = flow through current x unit load
CL = output load capacitance
D = duty cycle of input high
fo = output frequency
fi = input frequency

PARAMETER MEASUREMENT INFORMATION



NOTES:

1. VOLP is measured with respect to a ground reference near the output under test. VOHV is measured with respect to VOH.
2. Input pulses have the following characteristics: PRR ≤ 1MHz, tr = 2.5ns, tf = 2.5ns, skew 1ns.
3. R.F. fixture with 700-MHz design rules required. IC should be soldered into test board and bypassed with 0.1μF capacitor. Scope and probes require 700-MHz bandwidth.

Figure 1 - Simultaneous switching transient waveforms.

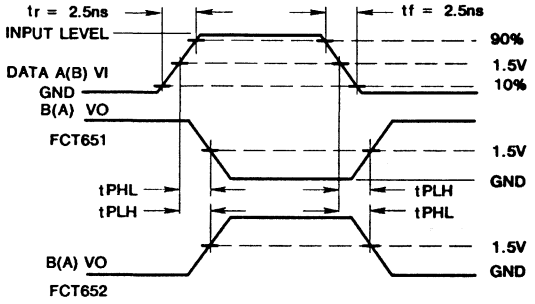


Figure 2 - Propagation delay times.

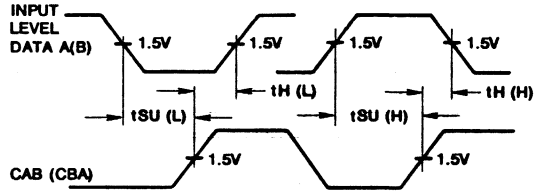
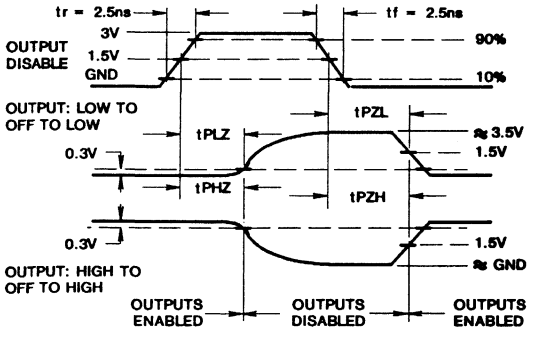
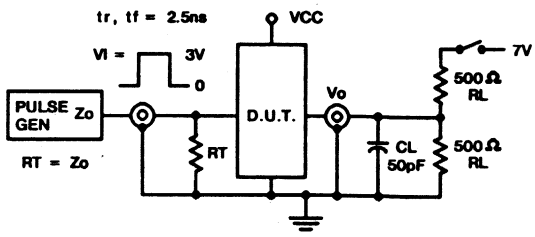


Figure 3 - Data setup and hold times.

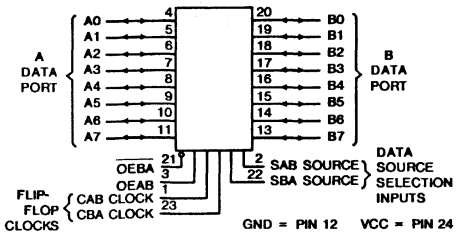




TEST	SWITCH POSITION
tPLZ, tPZL, OPEN DRAIN	CLOSED
tPHZ, tPZH, tPLH, tPHL	OPEN

Figure 4 - Three-state propagation delay times and test circuit.

CD54/74FCT653, CD54/74FCT654



FUNCTIONAL DIAGRAM

Octal Bus Transceivers/ Registers, Open-Drain (A Side), 3-State (B Side)

CD54/74FCT653 - Inverting
CD54/74FCT654 - Non-Inverting

Type Features:

- *Buffered inputs*
- *Typical propagation delay: 3.5ns @ VCC = 5V, TA = 25°C, CL = 50pF*

Family Features:

- *SCR-latchup-resistant CMOS process and circuit design*
- *Speed of bipolar FAST*/AS/S with significantly reduced power consumption*
- *64/48-mA output sink current (commercial/extended industrial)*
- *Output voltage swing limited to 3.7V @ VCC = 5V*
- *Controlled output-edge rates*
- *Input/output isolation to VCC*
- *BiMOS technology with low quiescent power*

* FAST is a registered trademark of Fairchild Semiconductor Corp.

The CD54/74FCT653 and CD54/74FCT654 octal bus transceivers/registers use a small-geometry BiMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output-HIGH level to two diode drops below VCC. This resultant lowering of output swing (0V to 3.7V) reduces power bus ringing (a source of EMI) and minimizes VCC bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enchances switching speed and is capable of sinking 48 to 64 milliamperes.

The CD54/74FCT653 is an inverting type having open drains on the A output and 3-state outputs on the B side. The CD54/74FCT654 differs only in that it is a non-inverting type. These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Output Enables OEAB and $\overline{\text{OEBA}}$ are provided to control the transceiver functions. SAB and SBA control pins are provided to select whether real-time or stored data is transferred. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A LOW input level selects real-time data, and a HIGH selects stored data. The following examples demonstrate the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers.

Data on the A or B data bus, or both, can be stored in the internal D flip-flops by low-to-high transistions at the appropriate clock pins (CAB or CBA) regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and $\overline{\text{OEBA}}$. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

The CD54/74FCT653 and CD54/74FCT654 are supplied in 24-lead dual-in-line narrow-body plastic packages (EN suffix) and in 24-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over two temperature ranges: Commercial (0°C to +70°C) and Extended Industrial (-55°C to +125°C).

The CD54FCT653 and CD54FCT654 are also available in chip form (H suffix). These unpackaged devices are operable over the -55°C to +125°C temperature range.

Printed in USA/8-89

File Number **2403**

FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION	
OEAB	$\overline{OEBA}$	CAB	CBA	SAB	SBA	A0 THRU A7	B0 THRU B7	CD54/74FCT653	CD54/74FCT654
L	H	H or L	H or L	X	X	Input	Input	Isolation *	Isolation *
L	H	⎍	⎍	X	X	Input	Input	Store A and B Data	Store A and B Data
X	H	⎍	H or L	X	X	Input	Unspecified †	Store A, Hold B	Store A, Hold B
H	H	⎍	⎍	X‡	X	Input	Output	Store A in both registers	Store A in both registers
L	X	H or L	⎍	X	X	Unspecified †	Input	Hold A, Store B	Hold, A Store B
L	L	⎍	⎍	X	X‡	Output	Input	Store B in both registers	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-Time $\overline{B}$ Data to A Bus	Real-Time B Data to A Bus
L	L	X	H or L	X	H	Output	Input	Stored $\overline{B}$ Data to A Bus	Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time $\overline{A}$ Data to B Bus	Real-Time A Data to B Bus
H	H	H or L	X	H	X	Input	Output	Stored $\overline{A}$ Data to B Bus	Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored $\overline{A}$ Data to B Bus Stored $\overline{B}$ Data to A Bus	Stored A Data to B Bus Stored B Data to A Bus

* To prevent excess currents in the High-Z (isolation) modes, all I/O terminals should be terminated with 10kΩ to 1MΩ resistors.

† The data output functions may be enabled or disabled by various signals at the OEAB or $\overline{OEBA}$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

‡ Select control = L: clocks can occur simultaneously.
Select control = H: clocks must be staggered in order to load both registers.

3

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (VCC) ..... -0.5V to 6V
DC INPUT DIODE CURRENT, IIK (for VI < -0.5V) ..... -20mA
DC OUTPUT DIODE CURRENT, IOK (for VO < -0.5V) ..... -50mA
DC OUTPUT SINK CURRENT per Output Pin, IO ..... +70mA
DC OUTPUT SOURCE CURRENT per Output Pin, IO ..... -30mA
DC VCC CURRENT (ICC) 140mA
DC GROUND CURRENT (IGND) 528mA
POWER DISSIPATION PER PACKAGE (PD):
For TA = -55°C to +100°C (PACKAGE TYPE E) 500mW
For TA = +100°C to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8mW/°C to 300mW
For TA = -55°C to +70°C (PACKAGE TYPE M) 400mW
For TA = +70°C to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 8mW/°C to 70mW
OPERATING-TEMPERATURE RANGE (TA):
PACKAGE TYPE E, M ..... -55°C to +125°C
STORAGE TEMPERATURE (Tstg) ..... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 in. ± 1/32 in. (1.59mm ± 0.79mm) from case for 10s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59mm) with solder contacting lead tips only ..... +300°C

RECOMMENDED OPERATING CONDITIONS:

The following are normal operating ranges for these devices. For maximum reliability, devices should always be operated within these ranges.

CHARACTERISTIC		LIMITS MIN	LIMITS MAX	UNITS
Supply-Voltage Range, VCC*:	CD74 Series, TA = 0°C to 70°C	4.75	5.25	V
	CD54 Series, TA = -55°C to +125°C	4.5	5.5	V
DC Input Voltage, VI		0	VCC	V
DC Output Voltage, VO		0	≤ VCC	V
Operating Temperature, TA		-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv		0	10	ns/V

* Unless otherwise specified, all voltages are referenced to ground.

STATIC ELECTRICAL CHARACTERISTICS

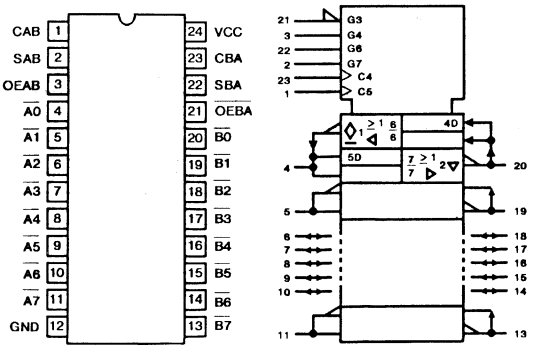
FCT Series: 74FCT Commercial Temperature Range, 0°C to +70°C; VCC max = 5.25V, VCC min = 4.75V
54FCT Extended Industrial Temperature Range, -55°C to +125°C; VCC max = 5.5V, VCC min = 4.5V

CHARACTERISTICS		TEST CONDITIONS VI (V)	IO (mA)	VCC (V)	AMBIENT TEMPERATURE (TA) +25°C MIN	+25°C MAX	0°C to +70°C MIN	0°C to +70°C MAX	-55°C to +125°C MIN	-55°C to +125°C MAX	UNITS
High-Level Input Voltage	VIH			4.5 to 5.5	2	-	2	-	2	-	V
Low-Level Input Voltage	VIL			4.5 to 5.5	-	0.8	-	0.8	-	0.8	V
High-Level Output Voltage	VOH	VIH or	-15	MIN	2.4	-	2.4	-	-	-	V
		VIL	-12	MIN	2.4	-	-	-	2.4	-	V
Low-Level Output Voltage	VOL	VIH or	64	MIN	-	0.55	-	0.55	-	-	V
		VIL	48	MIN	-	0.55	-	-	-	0.55	V
High-Level Input Current	IIH	VCC		MAX	-	0.1	-	1	-	1	µA
Low-Level Input Current	IIL	GND		MAX	-	-0.1	-	-1	-	-1	µA
3-State Leakage Current	IOZH	VCC		MAX	-	0.5	-	10	-	10	µA
	IOZL	GND		MAX	-	-0.5	-	-10	-	-10	µA
Short-Circuit Output Current *	IOS	VCC or GND VO = 0		MAX	-60	-	-60	-	-60	-	mA
Input Clamp Voltage	VIK	VCC or GND	-18	MIN	-	-1.2	-	-1.2	-	-1.2	V
Quiescent Supply Current, MSI	ICC	VCC or GND	0	MAX	-	8	-	80	-	500	µA
Additional Quiescent Supply Current per Input Pin TTL Inputs High, 1 Unit Load	ΔICC	3.4V†		MAX	-	1.6	-	1.6	-	2	mA

* Not more than one output should be shorted at one time. Test duration should not exceed 100ms.
† Inputs that are not measured are at VCC or GND.

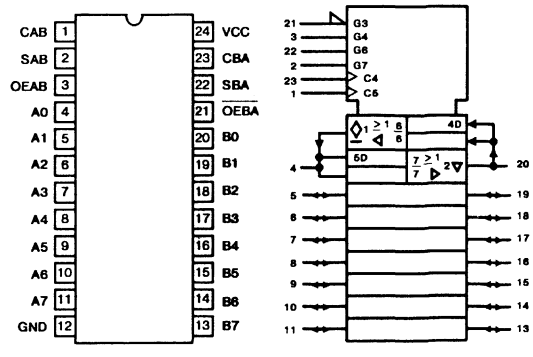
FCT Input Loading: All inputs are 1 unit load. Unit load is ΔICC limit specified in Static Characteristics Chart, e.g., 1.6mA max. @ +70°C.

CD54/74FCT653 TYPES



TERMINAL ASSIGNMENT — IEC LOGIC SYMBOL

CD54/74FCT654 TYPES



TERMINAL ASSIGNMENT — IEC LOGIC SYMBOL

PREREQUISITE FOR SWITCHING

CHARACTERISTICS	SYMBOL	VCC (V)	AMBIENT TEMPERATURE (TA) 0°C to +70°C MIN	0°C to +70°C MAX	-55°C to +125°C MIN	-55°C to +125°C MAX	UNITS
Maximum Frequency (B Side as Outputs)	fMAX	5†	80	-	80	-	MHz
Data to Clock Setup Time	tSU	5	4	-	4.5	-	ns
Data to Clock Hold Time	tH	5	2	-	2	-	ns
Clock Pulse Width	tW	5	6	-	6	-	ns

†5V: min. is @ 4.5V
5V: min. is @ 4.75V for 0°C to +70°C

SWITCHING CHARACTERISTICS

FCT Series: tr, tf = 2.5ns, CL = 50pF, RL - See Figures 3 and 4

CHARACTERISTICS		SYMBOL	VCC (V)	AMBIENT TEMPERATURE (TA) 0°C to +70°C MIN	0°C to +70°C MAX	-55°C to +125°C MIN	-55°C to +125°C MAX	UNITS
Propatagion Delays:								
Stored A Data to $\overline{B}$ Bus	FCT653	tPLH, tPHL	5†	2	9	2	10	ns
Stored A Data to B Bus	FCT654	tPLH, tPHL	5	2	9	2	10	ns
Stored $\overline{B}$ Data to A Bus	FCT653	tPZL	5	2	8	2	9	ns
		tPLZ	5	2	9	2	11	ns
Stored B Data to A Bus	FCT654	tPZL, tPLZ	5	2	9	2	11	ns
A Data to $\overline{B}$ Bus	FCT653	tPLH, tPHL	5	2	8	2	9	ns
A Data to B Bus	FCT654	tPLH, tPHL	5	2	9	2	11	ns
$\overline{B}$ Data to A Bus	FCT653	tPZL	5	2	8	2	9	ns
		tPLZ	5	2	9	2	11	ns
B Data to A Bus	FCT654	tPZL, tPLZ	5	2	9	2	11	ns
Select to Data (B Bus)	FCT653, FCT654	tPLH, tPHL	5	2	11	2	12	ns
Select to Data (A Bus)	FCT653	tPZL	5	2	8	2	9	ns
		tPLZ	5	2	9	2	11	ns
Select to Data (A Bus)	FCT654	tPZL, tPLZ	5	2	9	2	11	ns
3-State Enabling Times (B Bus) Bus to Output or Register to Output	FCT653	tPZL, tPZH	5	2	14	2	15	ns
	FCT654	tPZL, tPZH	5	2	15	2	18	ns
3-State Disabling Times (B Bus) Bus to Output or Register to Output	FCT653	tPLZ, tPHZ	5	2	9	2	11	ns
	FCT654	tPLZ, tPHZ	5	2	9	2	11	ns
Off-State Enabling Times (A Bus) Bus to Output or Register to Output	FCT653	tPZL	5	2	14	2	15	ns
	FCT654	tPZL	5	2	15	2	18	ns
Off-State Disabling Times (A Bus) Bus to Output or Register to Output	FCT653	tPLZ	5	2	9	2	11	ns
	FCT654	tPLZ	5	2	9	2	11	ns

†5V: min. is @ 5.5V
max. is @ 4.5V
5V: min. is @ 5.25V for 0°C to +70°C
max. is @ 4.75V for 0°C to +70°C

§CPD, measured per flip-flop, is used to determine the dynamic power consumption.
PD (per package) = VCC ICC + Σ (VCC^2 fi CPD + VO^2 fo CL + VCC ΔICCD) where:
VCC = supply voltage
ΔICC = flow through current x unit load
CL = output load capacitance
D = duty cycle of input high
fo = output frequency
fi = input frequency

SWITCHING CHARACTERISTICS (Continued)

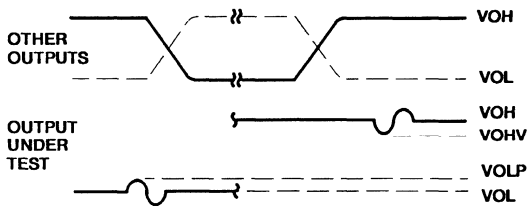
FCT Series: tr, tf = 2.5ns, CL = 50pF, RL - See Figure 3 and 4

CHARACTERISTICS	SYMBOL	VCC (V)	AMBIENT TEMPERATURE (TA) 0°C to +70°C MIN	0°C to +70°C MAX	-55°C to +125°C MIN	-55°C to +125°C MAX	UNITS
Power Dissipation Capacitance	CPD §	-					pF
Min. (Valley) VOH (B Side) During Switching of Other Outputs (Output Under Test Not Switching)	VOHV See Figure 1	5	0.5 Typical @ +25°C				V
Max. (Peak) VOL During Switching of Other Outputs (Output Under Test Not Switching)	VOLP See Figure 1	5	1 Typical @ +25°C				V
Input Capacitance	CI	-	-	10	-	10	pF
3-State Output Capacitance (B Side)	CO	-	-	15	-	15	pF
Off-State Output Capacitance (A Side)	CO	-	-	15	-	15	pF

†5V: min. is @ 5.5V
max. is @ 4.5V
5V: min. is @ 5.25V for 0°C to +70°C
max. is @ 4.75V for 0°C to +70°C

§CPD, measured per flip-flop, is used to determine the dynamic power consumption.
PD (per package) = VCC ICC + Σ (VCC² fi CPD + VO² fo CL + VCC ΔICCD) where:
VCC = supply voltage
ΔICC = flow through current x unit load
CL = output load capacitance
D = duty cycle of input high
fo = output frequency
fi = input frequency

PARAMETER MEASUREMENT INFORMATION



NOTES:
1. VOLP is measured with respect to a ground reference near the output under test. VOHV is measured with respect to VOH.
2. Input pulses have the following characteristics: PRR ≤ 1MHz, tr = 2.5ns, tf = 2.5ns, skew 1ns.
3. R.F. fixture with 700-MHz design rules required. IC should be soldered into test board and bypassed with 0.1μF capacitor. Scope and probes require 700-MHz bandwidth.

Figure 1 - Simultaneous switching transient waveforms.

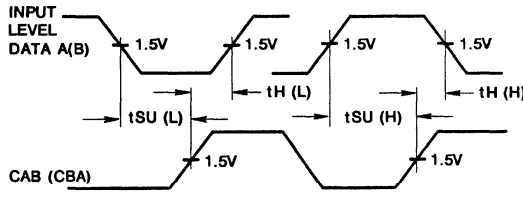
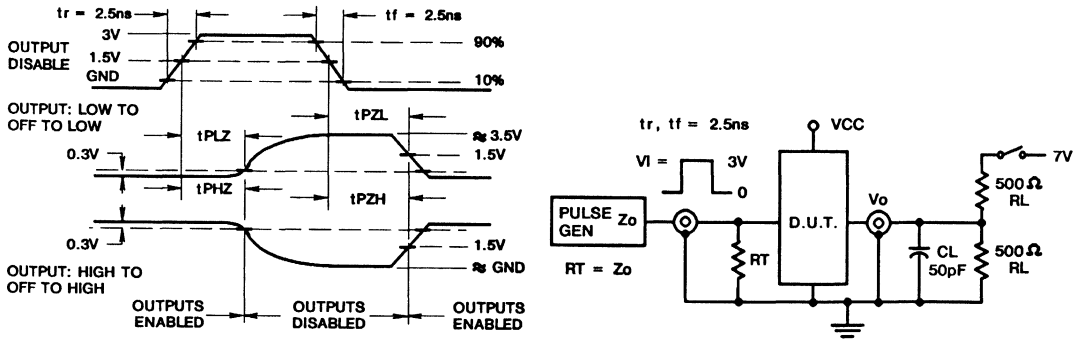


Figure 2 - Data setup and hold times.



TEST	SWITCH POSITION
tPLZ, tPZL, OPEN DRAIN	CLOSED
tPHZ, tPZH, tPLH, tPHL	OPEN

3

Figure 3 - Three-state propagation delay waveforms and test circuit (B outputs).

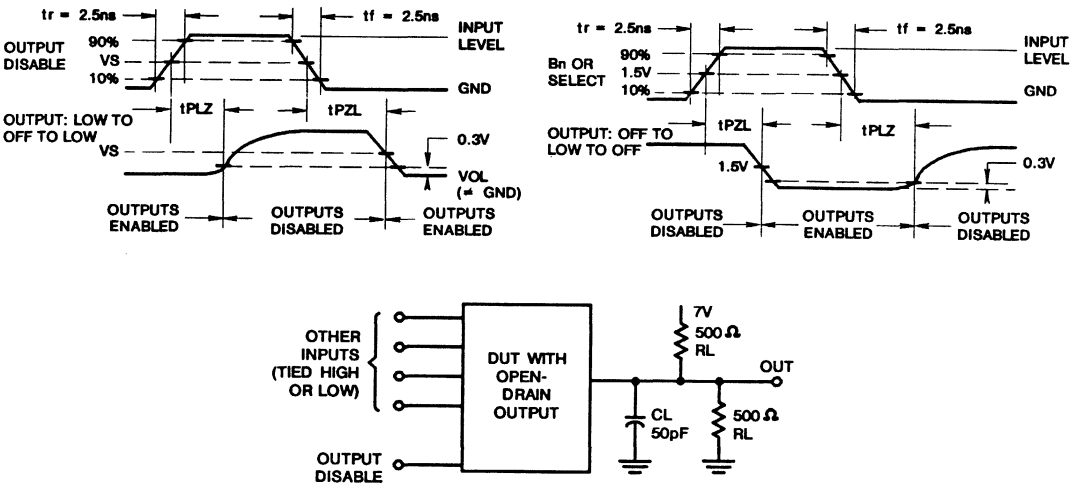
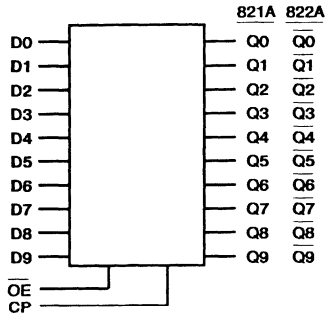


Figure 4 - Open-drain propagation delay times and test circuit (A outputs).

CD54/74FCT821A, CD54/74FCT822A



FUNCTIONAL DIAGRAM

10-Bit D-Type Flip-Flops, 3-State

Positive-Edge Triggered
CD54/74FCT821A - Non-Inverting
CD54/74FCT822A - Inverting

Type Features:

- *Buffered inputs*
- *Typical propagation delay: 3.5ns @ VCC = 5V, TA = +25°C, CL = 50pF*

The CD54/74FCT821A and CD54/74FCT822A 10-bit, D-type, 3-state, positive-edge-triggered flip-flops use a small-geometry BiMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output-HIGH level to two diode drops below VCC. This resultant lowering of output swing (0V to 3.7V) reduces power bus ringing (a source of EMI) and minimizes VCC bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 32 to 48 milliamperes.

The 10 flip-flops enter data into their registers on the LOW-to-HIGH transition of the clock (CP). The Output Enable ($\overline{OE}$) controls the 3-state outputs and is independent of the register operation. When the Output Enable ($\overline{OE}$) is HIGH, the outputs are in the high-impedance state. The CD54/74FCT821A and CD54/74FCT822A share the same configurations, but the CD54/74FCT821A outputs are non-inverted while the CD54/74FCT822A devices have inverted outputs.

The CD54/74FCT821A and CD54/74FCT822A are supplied in 24-lead dual-in-line narrow-body plastic packages (EN suffix) and in 24-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over two temperature ranges: Commercial (0°C to +70°C) and Extended Industrial (-55°C to +125°C).

The CD54FCT821A and CD54FCT822A are also available in chip form (H suffix). These unpackaged devices are operable over the -55°C to +125°C temperature range.

Family Features:

- *SCR-latchup-resistant CMOS process and circuit design*
- *Speed of bipolar FAST*/AS/S with significantly reduced power consumption*
- *48/32-mA output sink current (commercial/extended industrial)*
- *Output voltage swing limited to 3.7V @ VCC = 5V*
- *Controlled output-edge rates*
- *Input/output isolation to VCC*
- *BiMOS technology with low quiescent power*

* FAST is a registered trademark of Fairchild Semiconductor Corp.

TRUTH TABLE

INPUTS			OUTPUTS	
			FCT821A	FCT822A
$\overline{OE}$	CP	Dn	Qn	$\overline{Q}n$
L	⎍	H	H	L
L	⎍	L	L	H
L	L	X	NC	NC
H	X	X	Z	Z

H = HIGH level (steady state)
L = LOW level (steady state)
X = Immaterial
⎍ = Transition from LOW to HIGH level
Z = HIGH impedance
NC = No change

Printed in USA/8-89

File Number **2390**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (VCC) ..... -0.5V to 6V
DC INPUT DIODE CURRENT, IIK (for VI < -0.5V) ..... -20mA
DC OUTPUT DIODE CURRENT, IOK (for VO < -0.5V) ..... -50mA
DC OUTPUT SINK CURRENT per Output Pin, IO ..... +70mA
DC OUTPUT SOURCE CURRENT per Output Pin, IO ..... -30mA
DC VCC CURRENT (ICC) 260mA
DC GROUND CURRENT (IGND) 500mA
POWER DISSIPATION PER PACKAGE (PD):
For TA = -55°C to +100°C (PACKAGE TYPE E) 500mW
For TA = +100°C to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8mW/°C to 300mW
For TA = -55°C to +70°C (PACKAGE TYPE M) 400mW
For TA = +70°C to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6mW/°C to 70mW
OPERATING-TEMPERATURE RANGE (TA):
PACKAGE TYPE E, M ..... -55°C to +125°C
STORAGE TEMPERATURE (Tstg) ..... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 in. ± 1/32 in. (1.59mm ± 0.79mm) from case for 10s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59mm) with solder contacting lead tips only ..... +300°C

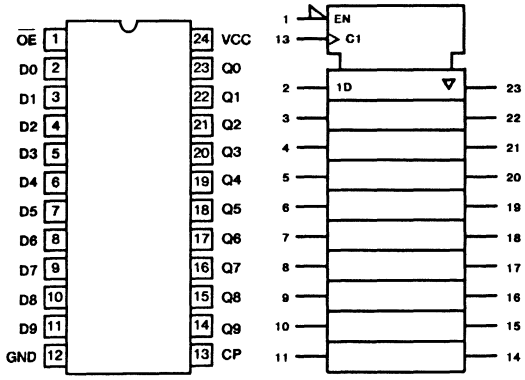
RECOMMENDED OPERATING CONDITIONS:

The following are normal operating ranges for these devices. For maximum reliability, devices should always be operated within these ranges.

CHARACTERISTIC		LIMITS MIN	LIMITS MAX	UNITS
Supply-Voltage Range, VCC*:	CD74 Series, TA = 0°C to 70°C	4.75	5.25	V
	CD54 Series, TA = -55°C to +125°C	4.5	5.5	V
DC Input Voltage, VI		0	VCC	V
DC Output Voltage, VO		0	≤ VCC	V
Operating Temperature, TA		-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv		0	10	ns/V

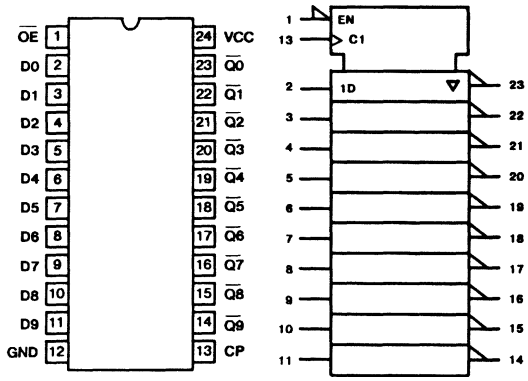
* Unless otherwise specified, all voltages are referenced to ground.

CD54/74FCT821A TYPES



TERMINAL ASSIGNMENT IEC LOGIC SYMBOL

CD54/74FCT822A TYPES



TERMINAL ASSIGNMENT IEC LOGIC SYMBOL

STATIC ELECTRICAL CHARACTERISTICS

FCT Series: 74FCT Commercial Temperature Range, 0°C to +70°C; VCC max = 5.25V, VCC min = 4.75V
54FCT Extended Industrial Temperature Range, -55°C to +125°C; VCC max = 5.5V, VCC min = 4.5V

CHARACTERISTICS		TEST CONDITIONS			AMBIENT TEMPERATURE (TA)						UNITS
					+25°C		0°C to +70°C		-55°C to +125°C		
		VI (V)	IO (mA)	VCC (V)	MIN	MAX	MIN	MAX	MIN	MAX	
High-Level Input Voltage	VIH			4.5 to 5.5	2	-	2	-	2	-	V
Low-Level Input Voltage	VIL			4.5 to 5.5	-	0.8	-	0.8	-	0.8	V
High-Level Output Voltage	VOH	VIH or	-24	MIN	2.4	-	2.4	-	-	-	V
		VIL	-20	MIN	2.4	-	-	-	2.4	-	V
Low-Level Output Voltage	VOL	VIH or	48	MIN	-	0.55	-	0.55	-	-	V
		VIL	32	MIN	-	0.55	-	-	-	0.55	V
High-Level Input Current	IIH	VCC		MAX	-	0.1	-	1	-	1	µA
Low-Level Input Current	IIL	GND		MAX	-	-0.1	-	-1	-	-1	µA
3-State Leakage Current	IOZH	VCC		MAX	-	0.5	-	10	-	10	µA
	IOZL	GND		MAX	-	-0.5	-	-10	-	-10	µA
Short-Circuit Output Current *	IOS	VCC or GND VO = 0		MAX	-60	-	-60	-	-60	-	mA
Input Clamp Voltage	VIK	VCC or GND	-18	MIN	-	-1.2	-	-1.2	-	-1.2	V
Quiescent Supply Current, MSI	ICC	VCC or GND	0	MAX	-	8	-	80	-	500	µA
Additional Quiescent Supply Current per Input Pin TTL Inputs High, 1 Unit Load	ΔICC	3.4V†		MAX	-	1.6	-	1.6	-	2	mA

* Not more than one output should be shorted at one time. Test duration should not exceed 100ms.
† Inputs that are not measured are at VCC or GND.

FCT Input Loading: All inputs are 1 unit load. Unit load is ΔICC limit specified in Static Characteristics Chart, e.g., 1.6mA max. @ +70°C.

PREREQUISITE FOR SWITCHING

CHARACTERISTICS	SYMBOL	VCC (V)	AMBIENT TEMPERATURE (TA) 0°C to +70°C MIN	0°C to +70°C MAX	-55°C to +125°C MIN	-55°C to +125°C MAX	UNITS
Clock Pulse Width	tW	5†	7	-	7	-	ns
Data to Clock Setup Time	tSU	5	4	-	4	-	ns
Data to Clock Hold Time	tH	5	2	-	2	-	ns
Maximum Clock Frequency	fMAX	5	70	-	60	-	MHz

†5V: min. is @ 4.5V
5V: min. is @ 4.75V for 0°C to +70°C

SWITCHING CHARACTERISTICS

FCT Series: tr, tf = 2.5ns, CL = 50pF, RL - See Figure 4

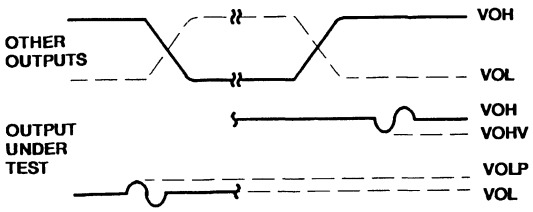
CHARACTERISTICS		SYMBOL	VCC (V)	AMBIENT TEMPERATURE (TA) 0°C to +70°C MIN	0°C to +70°C MAX	-55°C to +125°C MIN	-55°C to +125°C MAX	UNITS
Propagation Delays:								
Clock to Q	FCT821A	tPLH, tPHL	5†	1.5	12	1.5	12	ns
Clock to $\overline{Q}$	FCT822A	tPLH, tPHL	5	1.5	12	1.5	12	ns
Output Enable to Q	FCT821A	tPZL, tPZH	5	1.5	14	1.5	15	ns
Output Disable to Q	FCT821A	tPLZ, tPHZ	5	1.5	16	1.5	18	ns
Output Enable to $\overline{Q}$	FCT822A	tPZL, tPZH	5	1.5	14	1.5	15	ns
Output Disable to $\overline{Q}$	FCT822A	tPLZ, tPHZ	5	1.5	16	1.5	18	ns
Power Dissipation Capacitance		CPD§	-					pF
Min. (Valley) VOHV During Switching of Other Outputs (Output Under Test Not Switching)		VOHV See Figure 1	5	0.5 Typical @ +25°C				V
Max. (Peak) VOLP During Switching of Other Outputs (Output Under Test Not Switching)		VOLP See Figure 1	5	1 Typical @ +25°C				V
Input Capacitance		CI	-	-	10	-	10	pF
3-State Output Capacitance		CO	-	-	15	-	15	pF

†5V: min. is @ 5.5V
max. is @ 4.5V
5V: min. is @ 5.25V for 0°C to +70°C
max. is @ 4.75V for 0°C to +70°C

§CPD, measured per flip-flop, is used to determine the dynamic power consumption.
PD (per package) = VCC ICC + Σ (VCC² fi CPD + VO² fo CL + VCC ΔICC D) where:
VCC = supply voltage
ΔICC = flow through current x unit load
CL = output load capacitance
D = duty cycle of input high
fo = output frequency
fi = input frequency

3

PARAMETER MEASUREMENT INFORMATION



NOTES:

1. VOLP is measured with respect to a ground reference near the output under test. VOHV is measured with respect to VOH.
2. Input pulses have the following characteristics: PRR $\leq$ 1MHz, tr = 2.5ns, tf = 2.5ns, skew 1ns.
3. R.F. fixture with 700-MHz design rules required. IC should be soldered into test board and bypassed with 0.1µF capacitor. Scope and probes require 700-MHz bandwidth.

Figure 1 - Simultaneous switching transient waveforms.

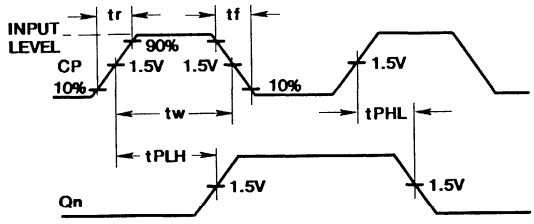


Figure 2 - Propagation delay times.

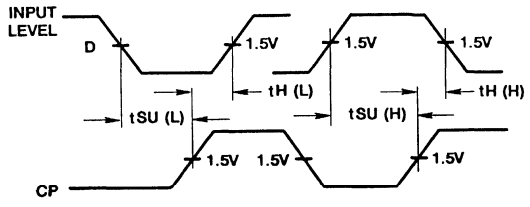
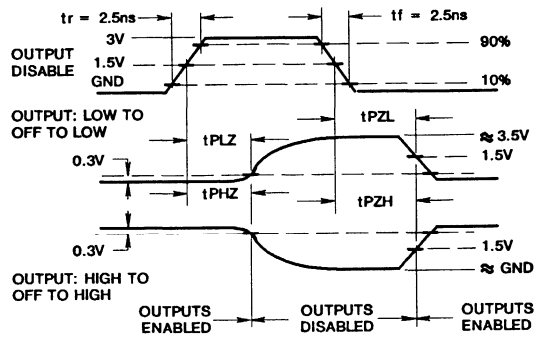
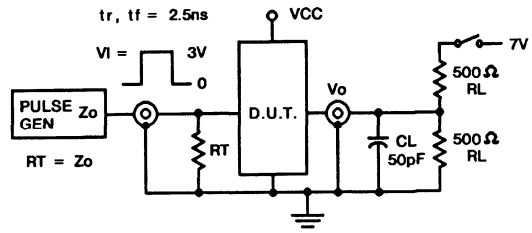


Figure 3 - Setup and hold times.

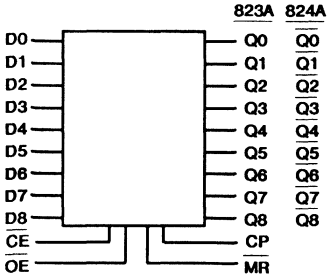




TEST	SWITCH POSITION
tPLZ, tPZL, OPEN DRAIN	CLOSED
tPHZ, tPZH, tPLH, tPHL	OPEN

Figure 4 - Three-state propagation delay times and test circuit.

CD54/74FCT823A, CD54/74FCT824A



FUNCTIONAL DIAGRAM

9-Bit D-Type Flip-Flops, 3-State

Positive-Edge-Triggered

CD54/74FCT823A - Non-Inverting
CD54/74FCT824A - Inverting

Type Features:

- *Buffered inputs*
- *Typical propagation delay: 3.5ns @ VCC = 5V, TA = 25°C, CL = 50pF*

3

The CD54/74FCT823A and CD54/74FCT824A 9-bit, D-type, 3-state, positive-edge-triggered flip-flops use a small-geometry BiMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output-HIGH level to two diode drops below VCC. This resultant lowering of output swing (0 to 3.7V) reduces power bus ringing (a source of EMI) and minimizes VCC bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 32 to 48 milliamperes.

The nine flip-flops enter data into their registers on the LOW-to-HIGH transition of the clock (CP). The Output Enable ($\overline{OE}$) controls the 3-state outputs and is independent of the register operation. These 9-bit-wide buffered registers with Clock Enable ($\overline{CE}$) and Master Reset ($\overline{MR}$) inputs are ideal for parity bus interfacing in high-performance microprogrammed systems.

The CD54/74FCT823A and CD54/74FCT824A are supplied in 24-lead dual-in-line narrow-body plastic packages (EN suffix) and in 24-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over two temperature ranges: Commercial (0 to +70°C) and Extended Industrial (-55°C to +125°C).

The CD54FCT823A and CD54FCT824A are also available in chip form (H suffix). These unpackaged devices are operable over the -55°C to +125°C temperature range.

Family Features:

- *SCR-latchup-resistant CMOS process and circuit design*
- *Speed of bipolar FAST*/AS/S with significantly reduced power consumption*
- *48/32-mA output sink current (commercial/extended industrial)*
- *Output voltage swing limited to 3.7V @ VCC = 5V*
- *Controlled output-edge rates*
- *Input/output isolation to VCC*
- *BiMOS technology with low quiescent power*

* FAST is a registered trademark of Fairchild Semiconductor Corp.

TRUTH TABLE

INPUTS					Q OUTPUTS		
$\overline{OE}$	$\overline{MR}$	$\overline{CE}$	D	CP	823A	824A	FUNCTION
H	X	L	L	⎍	Z	Z	High Z
H	X	L	H	⎍	Z	Z	
H	L	X	X	X	Z	Z	Reset
L	L	X	X	X	L	L	
H	H	H	X	X	Z	Z	Hold
L	H	H	X	X	NC	NC	
H	H	L	L	⎍	Z	Z	Load
H	H	L	H	⎍	Z	Z	
L	H	L	L	⎍	L	H	
L	H	L	H	⎍	H	L	

H = HIGH, L = LOW, X = Don't Care, NC = No Change,
⎍ = LOW-to-HIGH transition, Z = High Impedance

Printed in USA/8-89

File Number **2389**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (VCC) ..... -0.5V to 6V
DC INPUT DIODE CURRENT, IIK (for VI < -0.5V) ..... -20mA
DC OUTPUT DIODE CURRENT, IOK (for VO < -0.5V) ..... -50mA
DC OUTPUT SINK CURRENT per Output Pin, IO ..... +70mA
DC OUTPUT SOURCE CURRENT per Output Pin, IO ..... -30mA
DC VCC CURRENT (ICC) 234mA
DC GROUND CURRENT (IGND) 453mA
POWER DISSIPATION PER PACKAGE (PD):
For TA = -55°C to +100°C (PACKAGE TYPE E) 500mW
For TA = +100°C to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8mW/°C to 300mW
For TA = -55°C to +70°C (PACKAGE TYPE M) 400mW
For TA = +70°C to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6mW/°C to 70mW
OPERATING-TEMPERATURE RANGE (TA):
PACKAGE TYPE E, M ..... -55°C to +125°C
STORAGE TEMPERATURE (Tstg) ..... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 in. ± 1/32 in. (1.59mm ± 0.79mm) from case for 10s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59mm) with solder contacting lead tips only ..... +300°C

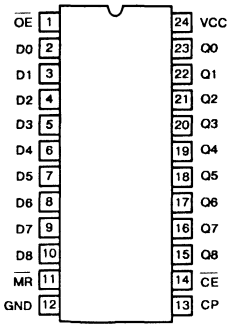
RECOMMENDED OPERATING CONDITIONS:

The following are normal operating ranges for these devices. For maximum reliability, devices should always be operated within these ranges.

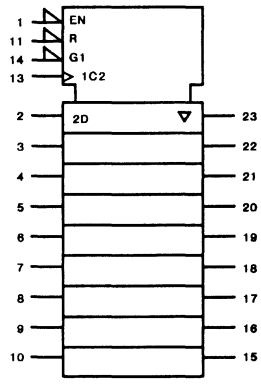
CHARACTERISTIC		LIMITS MIN	LIMITS MAX	UNITS
Supply-Voltage Range, VCC*:	CD74 Series, TA = 0°C to 70°C	4.75	5.25	V
	CD54 Series, TA = -55°C to +125°C	4.5	5.5	V
DC Input Voltage, VI		0	VCC	V
DC Output Voltage, VO		0	≤ VCC	V
Operating Temperature, TA		-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv		0	10	ns/V

* Unless otherwise specified, all voltages are referenced to ground.

CD54/74FCT823A

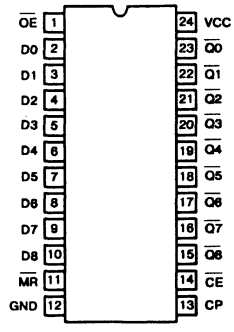


TERMINAL ASSIGNMENT

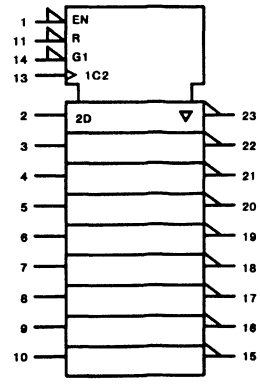


IEC LOGIC SYMBOL

CD54/74FCT824A



TERMINAL ASSIGNMENT



IEC LOGIC SYMBOL

STATIC ELECTRICAL CHARACTERISTICS

FCT Series: 74FCT Commercial Temperature Range, 0°C to +70°C; VCC max = 5.25V, VCC min = 4.75V
54FCT Extended Industrial Temperature Range, -55°C to +125°C; VCC max = 5.5V, VCC min = 4.5V

CHARACTERISTICS		TEST CONDITIONS VI (V)	TEST CONDITIONS IO (mA)	VCC (V)	AMBIENT TEMPERATURE (TA) +25°C MIN	+25°C MAX	0°C to +70°C MIN	0°C to +70°C MAX	-55°C to +125°C MIN	-55°C to +125°C MAX	UNITS
High-Level Input Voltage	VIH			4.5 to 5.5	2	-	2	-	2	-	V
Low-Level Input Voltage	VIL			4.5 to 5.5	-	0.8	-	0.8	-	0.8	V
High-Level Output Voltage	VOH	VIH or	-24	MIN	2.4	-	2.4	-	-	-	V
		VIL	-20	MIN	2.4	-	-	-	2.4	-	V
Low-Level Output Voltage	VOL	VIH or	48	MIN	-	0.55	-	0.55	-	-	V
		VIL	32	MIN	-	0.55	-	-	-	0.55	V
High-Level Input Current	IIH	VCC		MAX	-	0.1	-	1	-	1	µA
Low-Level Input Current	IIL	GND		MAX	-	-0.1	-	-1	-	-1	µA
3-State Leakage Current	IOZH	VCC		MAX	-	0.5	-	10	-	10	µA
	IOZL	GND		MAX	-	-0.5	-	-10	-	-10	µA
Short-Circuit Output Current *	IOS	VCC or GND VO = 0		MAX	-60	-	-60	-	-60	-	mA
Input Clamp Voltage	VIK	VCC or GND	-18	MIN	-	-1.2	-	-1.2	-	-1.2	V
Quiescent Supply Current, MSI	ICC	VCC or GND	0	MAX	-	8	-	80	-	500	µA
Additional Quiescent Supply Current per Input Pin TTL Inputs High, 1 Unit Load	ΔICC	3.4V†		MAX	-	1.6	-	1.6	-	2	mA

* Not more than one output should be shorted at one time. Test duration should not exceed 100ms.
† Inputs that are not measured are at VCC or GND.

FCT Input Loading: All inputs are 1 unit load. Unit load is ΔICC limit specified in Static Characteristics Chart, e.g., 1.6mA max. @ +70°C.

PREREQUISITE FOR SWITCHING

CHARACTERISTICS	SYMBOL	VCC (V)	AMBIENT TEMPERATURE (TA)				UNITS
			0°C to +70°C		-55°C to +125°C		
			MIN	MAX	MIN	MAX	
Pulse Width — Clock, $\overline{MR}$	tW	5†	7	-	7	-	ns
Setup Time — Data to Clock, $\overline{CE}$ to Clock	tSU	5	4	-	4	-	ns
Hold Time — Data, $\overline{CE}$	tH	5	2	-	2	-	ns
Master Reset Recovery Time	tREC	5	7	-	7	-	ns
Maximum Clock Frequency	fMAX	5	70	-	60	-	MHz

†5V: min. is @ 4.5V
5V: min. is @ 4.75V for 0°C to +70°C

SWITCHING CHARACTERISTICS

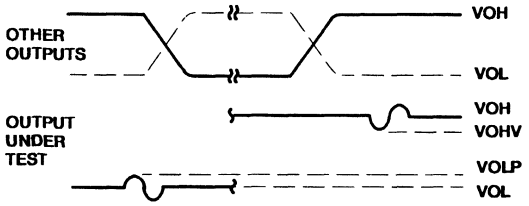
FCT Series: tr, tf = 2.5ns, CL = 50pF, RL - See Figure 4

CHARACTERISTICS		SYMBOL	VCC (V)	AMBIENT TEMPERATURE (TA)				UNITS
				0°C to +70°C		-55°C to +125°C		
				MIN	MAX	MIN	MAX	
Propagation Delays:								
Clock to Q	FCT823A	tPLH, tPHL	5†	1.5	12	1.5	12	ns
Clock to $\overline{Q}$	FCT824A	tPLH, tPHL	5	1.5	12	1.5	12	ns
$\overline{MR}$ to Q		tPHL	5	1.5	20	1.5	20	ns
Output Enable to Q	FCT823A	tPZL, tPZH	5	1.5	14	1.5	15	ns
Output Disable to Q	FCT823A	tPLZ, tPHZ	5	1.5	16	1.5	18	ns
Output Enable to $\overline{Q}$	FCT824A	tPZL, tPZH	5	1.5	14	1.5	15	ns
Output Disable to $\overline{Q}$	FCT824A	tPLZ, tPHZ	5	1.5	16	1.5	18	ns
Power Dissipation Capacitance		CPD§	-					pF
Min. (Valley) VOHV During Switching of Other Outputs (Output Under Test Not Switching)		VOHV See Figure 1	5	0.5 Typical @ +25°C				V
Max. (Peak) VOLP During Switching of Other Outputs (Output Under Test Not Switching)		VOLP See Figure 1	5	1 Typical @ +25°C				V
Input Capacitance		CI	-	-	10	-	10	pF
3-State Output Capacitance		CO	-	-	15	-	15	pF

†5V: min. is @ 5.5V
max. is @ 4.5V
5V: min. is @ 5.25V for 0°C to +70°C
max. is @ 4.75V for 0°C to +70°C

§CPD, measured per flip-flop, is used to determine the dynamic power consumption.
PD (per package) = VCC ICC + Σ (VCC^2 fi CPD + VO^2 fo CL + VCC ΔICC D) where:
VCC = supply voltage
ΔICC = flow through current x unit load
CL = output load capacitance
D = duty cycle of input high
fo = output frequency
fi = input frequency

PARAMETER MEASUREMENT INFORMATION



NOTES:

1. VOLP is measured with respect to a ground reference near the output under test. VOHV is measured with respect to VOH.
2. Input pulses have the following characteristics: PRR $\leq$ 1MHz, tr = 2.5ns, tf = 2.5ns, skew 1ns.
3. R.F. fixture with 700-MHz design rules required. IC should be soldered into test board and bypassed with 0.1µF capacitor. Scope and probes require 700-MHz bandwidth.

Figure 1 - Simultaneous switching transient waveforms.

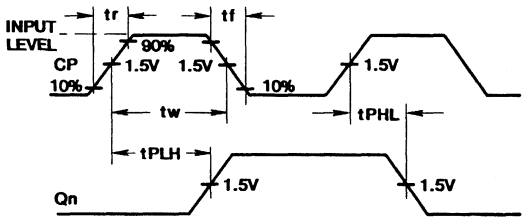


Figure 2 - propagation delay times.

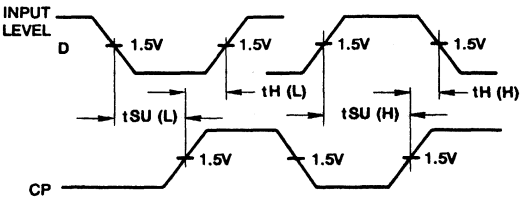
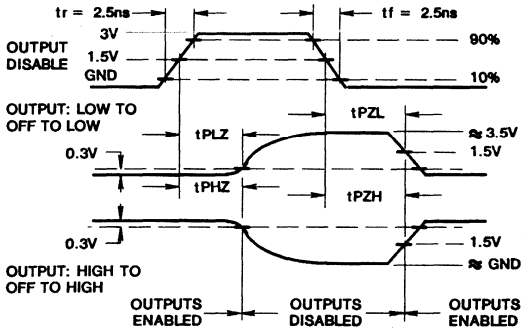
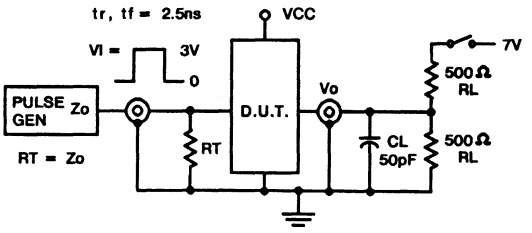


Figure 3 - setup and hold times.

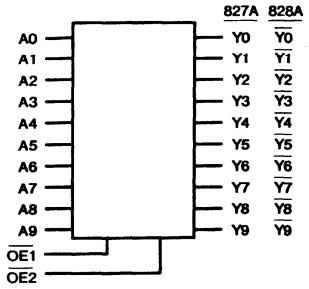




TEST	SWITCH POSITION
tPLZ, tPZL, OPEN DRAIN	CLOSED
tPHZ, tPZH, tPLH, tPHL	OPEN

Figure 4 - Three-state propagation delay times and test circuit.

CD54/74FCT827A, CD54/74FCT828A



FUNCTIONAL DIAGRAM

10-Bit Buffers/Line Drivers, 3-State

CD54/74FCT827A - Non-Inverting
CD54/74FCT828A - Inverting

Type Features:

- *Buffered inputs*
- *Typical propagation delay: 3.5ns @ VCC = 5V, TA = +25°C, CL = 50pF*

The CD54/74FCT827A and CD54/74FCT828A 10-bit, 3-state, bus drivers use small-geometry BiMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output-HIGH level to two diode drops below VCC. This resultant lowering of output swing (0V to 3.7V) reduces power bus ringing (a source of EMI) and minimizes VCC bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 32 to 48 milliamperes. These drivers provide high-performance bus interface buffering for wide data paths or buses carrying parity.

The CD54/74FCT827A and CD54/74FCT828A are supplied in 24-lead dual-in-line narrow-body plastic packages (EN suffix) and in 24-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over two temperature ranges: Commercial (0°C to +70°C) and Extended Industrial (-55°C to +125°C).

The CD54FCT827A and CD54FCT828A are also available in chip form (H suffix). These unpackaged devices are operable over the -55°C to +125°C temperature range.

Family Features:

- *SCR-latchup-resistant CMOS process and circuit design*
- *Speed of bipolar FAST*/AS/S with significantly reduced power consumption*
- *48/32-mA output sink current (commercial/extended industrial)*
- *Output voltage swing limited to 3.7V @ VCC = 5V*
- *Controlled output-edge rates*
- *Input/output isolation to VCC*
- *BiMOS technology with low quiescent power*

* FAST is a registered trademark of Fairchild Semiconductor Corp.

TRUTH TABLE

INPUTS			OUTPUTS	
			FCT827A	FCT828A
$\overline{OE1}$	$\overline{OE2}$	An	Yn	$\overline{Yn}$
L	L	L	L	H
L	L	H	H	L
H	X	X	Z	Z
X	H	X	Z	Z

H = HIGH Voltage Level (steady state)
L = LOW Voltage Level (steady state)
X = Immaterial
Z = HIGH Impedance

Printed in USA/8-89

File Number **2395**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (VCC) ..... -0.5V to 6V
DC INPUT DIODE CURRENT, IIK (for VI < -0.5V) ..... -20mA
DC OUTPUT DIODE CURRENT, IOK (for VO < -0.5V) ..... -50mA
DC OUTPUT SINK CURRENT per Output Pin, IO ..... +70mA
DC OUTPUT SOURCE CURRENT per Output Pin, IO ..... -30mA
DC VCC CURRENT (ICC) 264mA
DC GROUND CURRENT (IGND) 500mA
POWER DISSIPATION PER PACKAGE (PD):
For TA = -55°C to +100°C (PACKAGE TYPE E) 500mW
For TA = +100°C to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8mW/°C to 300mW
For TA = -55°C to +70°C (PACKAGE TYPE M) 400mW
For TA = +70°C to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6mW/°C to 70mW
OPERATING-TEMPERATURE RANGE (TA):
PACKAGE TYPE E, M ..... -55°C to +125°C
STORAGE TEMPERATURE (Tstg) ..... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 in. ± 1/32 in. (1.59mm ± 0.79mm) from case for 10s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59mm) with solder contacting lead tips only ..... +300°C

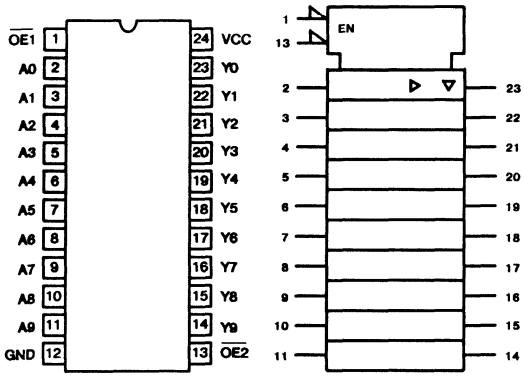
RECOMMENDED OPERATING CONDITIONS:

The following are normal operating ranges for these devices. For maximum reliability, devices should always be operated within these ranges.

CHARACTERISTIC		LIMITS MIN	LIMITS MAX	UNITS
Supply-Voltage Range, VCC*:	CD74 Series, TA = 0°C to 70°C	4.75	5.25	V
	CD54 Series, TA = -55°C to +125°C	4.5	5.5	V
DC Input Voltage, VI		0	VCC	V
DC Output Voltage, VO		0	≤ VCC	V
Operating Temperature, TA		-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv		0	10	ns/V

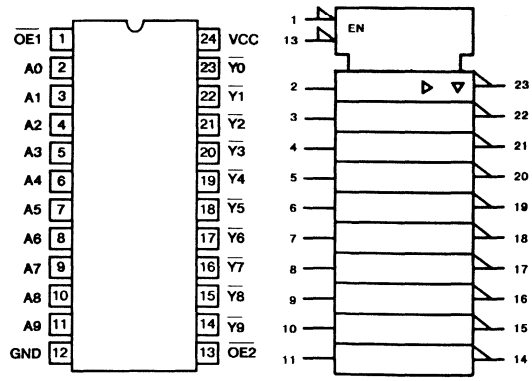
* Unless otherwise specified, all voltages are referenced to ground.

CD54/74FCT827A TYPES



TERMINAL ASSIGNMENT — IEC LOGIC SYMBOL

CD54/74FCT828A TYPES



TERMINAL ASSIGNMENT — IEC LOGIC SYMBOL

STATIC ELECTRICAL CHARACTERISTICS

FCT Series: 74FCT Commercial Temperature Range, 0°C to +70°C; VCC max = 5.25V, VCC min = 4.75V
54FCT Extended Industrial Temperature Range, -55°C to +125°C; VCC max = 5.5V, VCC min = 4.5V

CHARACTERISTICS		TEST CONDITIONS VI (V)	TEST CONDITIONS IO (mA)	VCC (V)	AMBIENT TEMPERATURE (TA) +25°C MIN	+25°C MAX	0°C to +70°C MIN	0°C to +70°C MAX	-55°C to +125°C MIN	-55°C to +125°C MAX	UNITS
High-Level Input Voltage	VIH			4.5 to 5.5	2	-	2	-	2	-	V
Low-Level Input Voltage	VIL			4.5 to 5.5	-	0.8	-	0.8	-	0.8	V
High-Level Output Voltage	VOH	VIH or	-24	MIN	2.4	-	2.4	-	-	-	V
		VIL	-20	MIN	2.4	-	-	-	2.4	-	V
Low-Level Output Voltage	VOL	VIH or	48	MIN	-	0.55	-	0.55	-	-	V
		VIL	32	MIN	-	0.55	-	-	-	0.55	V
High-Level Input Current	IIH	VCC		MAX	-	0.1	-	1	-	1	µA
Low-Level Input Current	IIL	GND		MAX	-	-0.1	-	-1	-	-1	µA
3-State Leakage Current	IOZH	VCC		MAX	-	0.5	-	10	-	10	µA
	IOZL	GND		MAX	-	-0.5	-	-10	-	-10	µA
Short-Circuit Output Current *	IOS	VCC or GND VO = 0		MAX	-60	-	-60	-	-60	-	mA
Input Clamp Voltage	VIK	VCC or GND	-18	MIN	-	-1.2	-	-1.2	-	-1.2	V
Quiescent Supply Current, MSI	ICC	VCC or GND	0	MAX	-	8	-	80	-	500	µA
Additional Quiescent Supply Current per Input Pin TTL Inputs High, 1 Unit Load	ΔICC	3.4V†		MAX	-	1.6	-	1.6	-	2	mA

* Not more than one output should be shorted at one time. Test duration should not exceed 100ms.
† Inputs that are not measured are at VCC or GND.

FCT Input Loading: All inputs are 1 unit load. Unit load is ΔICC limit specified in Static Characteristics Chart, e.g., 1.6mA max. @ +70°C.

SWITCHING CHARACTERISTICS

FCT Series: tr, tf = 2.5ns, CL = 50pF, RL - See Figure 3

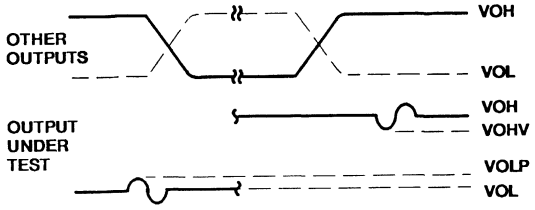
CHARACTERISTICS		SYMBOL	VCC (V)	AMBIENT TEMPERATURE (TA) 0°C to +70°C MIN	0°C to +70°C MAX	-55°C to +125°C MIN	-55°C to +125°C MAX	UNITS
Propagation Delays: Data to Outputs	FCT827A	tPLH, tPHL	5†	1.5	8	1.5	10	ns
	FCT828A	tPLH, tPHL	5	1.5	7.5	1.5	9.5	ns
Output Disable to Output		tPLZ, tPHZ	5	1.5	17	1.5	19	ns
Output Enable to Output		tPZH, tPZL	5	1.5	15	1.5	17	ns
Power Dissipation Capacitance		CPD§	-					pF
Min. (Valley) VOHV During Switching of Other Outputs (Output Under Test Not Switching)		VOHV See Figure 1	5	0.5 Typical @ +25°C				V
Max. (Peak) VOLP During Switching of Other Outputs (Output Under Test Not Switching)		VOLP See Figure 1	5	1 Typical @ +25°C				V
Input Capacitance		CI	-	-	10	-	10	pF
3-State Output Capacitance		CO	-	-	15	-	15	pF

†5V: min. is @ 5.5V
max. is @ 4.5V
5V: min. is @ 5.25V for 0°C to +70°C
max. is @ 4.75V for 0°C to +70°C

§CPD, measured per function, is used to determine the dynamic power consumption.
PD (per package) = VCC ICC + Σ (VCC^2 fi CPD + VO^2 fo CL + VCC ΔICC D) where:
VCC = supply voltage
ΔICC = flow through current x unit load
CL = output load capacitance
D = duty cycle of input high
fo = output frequency
fi = input frequency

3

PARAMETER MEASUREMENT INFORMATION



NOTES:

1. VOLP is measured with respect to a ground reference near the output under test. VOHV is measured with respect to VOH.
2. Input pulses have the following characteristics: PRR $\leq$ 1MHz, tr = 2.5ns, tf = 2.5ns, skew 1ns.
3. R.F. fixture with 700-MHz design rules required. IC should be soldered into test board and bypassed with 0.1µF capacitor. Scope and probes require 700-MHz bandwidth.

Figure 1 - Simultaneous switching transient waveforms.

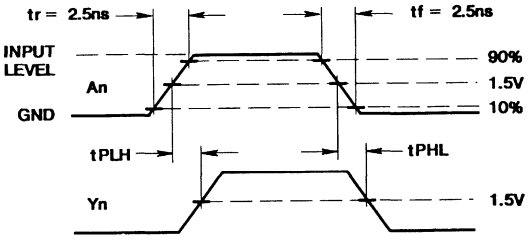
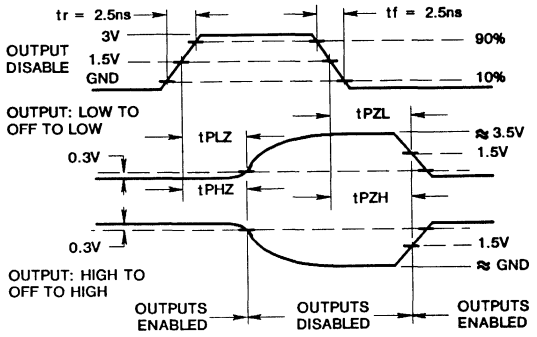
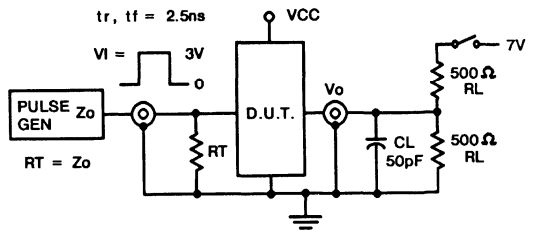


Figure 2 - Propagation delay times.

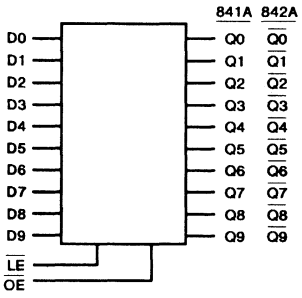




TEST	SWITCH POSITION
tPLZ, tPZL, OPEN DRAIN	CLOSED
tPHZ, tPZH, tPLH, tPHL	OPEN

Figure 3 - Three-state propagation delay times and test circuit.

CD54/74FCT841A, CD54/74FCT842A



FUNCTIONAL DIAGRAM

10-Bit Transparent Latch, 3-State

CD54/74FCT841A - Non-Inverting
CD54/74FCT842A - Inverting

Type Features:

- *Buffered inputs*
- *Typical propagation delay: 3.5ns @ VCC = 5V, TA = +25°C, CL = 50pF*

3

The CD54/74FCT841A and CD54/74FCT842A 10-bit transparent latches use a small-geometry BiMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output-HIGH level to two diode drops below VCC. This resultant lowering of output swing (0V to 3.7V) reduces power bus ringing (a source of EMI) and minimizes VCC bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 32 to 48 milliamperes.

The CD54/74FCT841A and CD54/74FCT842A outputs are transparent to the inputs when the Latch Enable ($\overline{LE}$) is HIGH. When the Latch Enable ($\overline{LE}$) goes LOW, the data is latched. The Output Enable ($\overline{OE}$) controls the 3-state outputs. When the Output Enable ($\overline{OE}$) is HIGH, the outputs are in the high-impedance state. The latch operation is independent of the state of the Output Enable. These devices provide extra data width for wider address/data paths or buses carrying parity.

The CD54/74FCT841A and CD54/74FCT842A are supplied in 24-lead dual-in-line narrow-body plastic packages (EN suffix) and in 24-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over two temperature ranges: Commercial (0°C to +70°C) and Extended Industrial (-55°C to +125°C).

The CD54FCT841A and CD54FCT842A are also available in chip form (H suffix). These unpackaged devices are operable over the -55°C to +125°C temperature range.

Family Features:

- *SCR-latchup-resistant CMOS process and circuit design*
- *Speed of bipolar FAST*/AS/S with significantly reduced power consumption*
- *48/32-mA output sink current (commercial/extended industrial)*
- *Output voltage swing limited to 3.7V @ VCC = 5V*
- *Controlled output-edge rates*
- *Input/output isolation to VCC*
- *BiMOS technology with low quiescent power*

* FAST is a registered trademark of Fairchild Semiconductor Corp.

TRUTH TABLE

$\overline{\text{OUTPUT ENABLE}}$	$\overline{\text{LATCH ENABLE}}$	DATA	FCT841A OUTPUT	FCT842A OUTPUT
L	H	H	H	L
L	H	L	L	H
L	L	l	L	H
L	L	h	H	L
H	X	X	Z	Z

H = HIGH voltage level
L = LOW voltage level
l = LOW voltage level one set-up time prior to the high-to-low latch enable transition.
h = HIGH voltage level one set-up time prior to the high-to-low latch enable transition.
X = Immaterial
Z = HIGH Impedance

Printed in USA/8-89

File Number **2397**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (VCC) ..... -0.5V to 6V
DC INPUT DIODE CURRENT, IIK (for VI < -0.5V) ..... -20mA
DC OUTPUT DIODE CURRENT, IOK (for VO < -0.5V) ..... -50mA
DC OUTPUT SINK CURRENT per Output Pin, IO ..... +70mA
DC OUTPUT SOURCE CURRENT per Output Pin, IO ..... -30mA
DC VCC CURRENT (ICC) 260mA
DC GROUND CURRENT (IGND) 500mA
POWER DISSIPATION PER PACKAGE (PD):
For TA = -55°C to +100°C (PACKAGE TYPE E) 500mW
For TA = +100°C to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8mW/°C to 300mW
For TA = -55°C to +70°C (PACKAGE TYPE M) 400mW
For TA = +70°C to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6mW/°C to 70mW
OPERATING-TEMPERATURE RANGE (TA):
PACKAGE TYPE E, M ..... -55°C to +125°C
STORAGE TEMPERATURE (Tstg) ..... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 in. ± 1/32 in. (1.59mm ± 0.79mm) from case for 10s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59mm) with solder contacting lead tips only ..... +300°C

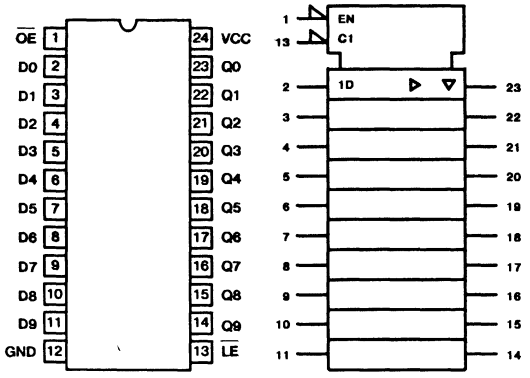
RECOMMENDED OPERATING CONDITIONS:

The following are normal operating ranges for these devices. For maximum reliability, devices should always be operated within these ranges.

CHARACTERISTIC		LIMITS MIN	LIMITS MAX	UNITS
Supply-Voltage Range, VCC*:	CD74 Series, TA = 0°C to 70°C	4.75	5.25	V
	CD54 Series, TA = -55°C to +125°C	4.5	5.5	V
DC Input Voltage, VI		0	VCC	V
DC Output Voltage, VO		0	≤ VCC	V
Operating Temperature, TA		-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv		0	10	ns/V

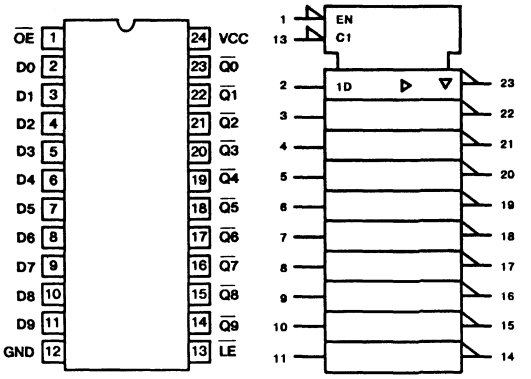
* Unless otherwise specified, all voltages are referenced to ground.

CD54/74FCT841A TYPES



TERMINAL ASSIGNMENT IEC LOGIC SYMBOL

CD54/74FCT842A TYPES



TERMINAL ASSIGNMENT IEC LOGIC SYMBOL

STATIC ELECTRICAL CHARACTERISTICS

FCT Series: 74FCT Commercial Temperature Range, 0°C to +70°C; VCC max = 5.25V, VCC min = 4.75V
54FCT Extended Industrial Temperature Range, -55°C to +125°C; VCC max = 5.5V, VCC min = 4.5V

CHARACTERISTICS		TEST CONDITIONS VI (V)	TEST CONDITIONS IO (mA)	VCC (V)	AMBIENT TEMPERATURE (TA) +25°C MIN	+25°C MAX	0°C to +70°C MIN	0°C to +70°C MAX	-55°C to +125°C MIN	-55°C to +125°C MAX	UNITS
High-Level Input Voltage	VIH			4.5 to 5.5	2	-	2	-	2	-	V
Low-Level Input Voltage	VIL			4.5 to 5.5	-	0.8	-	0.8	-	0.8	V
High-Level Output Voltage	VOH	VIH or	-24	MIN	2.4	-	2.4	-	-	-	V
		VIL	-20	MIN	2.4	-	-	-	2.4	-	V
Low-Level Output Voltage	VOL	VIH or	48	MIN	-	0.55	-	0.55	-	-	V
		VIL	32	MIN	-	0.55	-	-	-	0.55	V
High-Level Input Current	IIH	VCC		MAX	-	0.1	-	1	-	1	µA
Low-Level Input Current	IIL	GND		MAX	-	-0.1	-	-1	-	-1	µA
3-State Leakage Current	IOZH	VCC		MAX	-	0.5	-	10	-	10	µA
	IOZL	GND		MAX	-	-0.5	-	-10	-	-10	µA
Short-Circuit Output Current *	IOS	VCC or GND VO = 0		MAX	-60	-	-60	-	-60	-	mA
Input Clamp Voltage	VIK	VCC or GND	-18	MIN	-	-1.2	-	-1.2	-	-1.2	V
Quiescent Supply Current, MSI	ICC	VCC or GND	0	MAX	-	8	-	80	-	500	µA
Additional Quiescent Supply Current per Input Pin TTL Inputs High, 1 Unit Load	ΔICC	3.4V†		MAX	-	1.6	-	1.6	-	2	mA

* Not more than one output should be shorted at one time. Test duration should not exceed 100ms.
† Inputs that are not measured are at VCC or GND.

FCT Input Loading: All inputs are 1 unit load. Unit load is ΔICC limit specified in Static Characteristics Chart, e.g., 1.6mA max. @ +70°C.

PREREQUISITE FOR SWITCHING

CHARACTERISTICS	SYMBOL	VCC (V)	AMBIENT TEMPERATURE (TA) 0°C to +70°C MIN	0°C to +70°C MAX	-55°C to +125°C MIN	-55°C to +125°C MAX	UNITS
$\overline{LE}$ Pulse Width	fW	5†	6	-	6	-	ns
Data to $\overline{LE}$ Setup Time	tSU	5	2.5	-	2.5	-	ns
Data to $\overline{LE}$ Hold Time	tH	5	2.5	-	3	-	ns

†5V: min. is @ 4.5V
5V: min. is @ 4.75V for 0°C to +70°C

SWITCHING CHARACTERISTICS

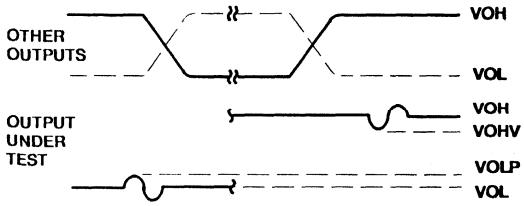
FCT Series: tr, tf = 2.5ns, CL = 50pF, RL - See Figure 4

CHARACTERISTICS		SYMBOL	VCC (V)	AMBIENT TEMPERATURE (TA) 0°C to +70°C MIN	0°C to +70°C MAX	-55°C to +125°C MIN	-55°C to +125°C MAX	UNITS
Propagation Delays: Data to Outputs	FCT841A	tPLH, tPHL	5†	1.5	9.5	1.5	11	ns
	FCT842A	tPLH, tPHL	5†	1.5	10	1.5	12	ns
$\overline{LE}$ to Outputs	FCT841A	tPLH, tPHL	5	2	12	2	16	ns
	FCT842A	tPLH, tPHL	5	2	12	2	16	ns
Output Enable Times	FCT841A	tPZL, tPZH	-	1.5	14	1.5	15	ns
	FCT842A	tPZL, tPZH	-	1.5	14	1.5	15	ns
Output Disable Times	FCT841A	tPLZ, tPHZ	-	1.5	12	1.5	12	ns
	FCT842A	tPLZ, tPHZ	-	1.5	12	1.5	12	ns
Power Dissipation Capacitance	FCT841A	CPD§	-					pF
	FCT842A	CPD§	-					pF
Min. (Valley) VOHV During Switching of Other Outputs (Output Under Test Not Switching)		VOHV See Figure 1	5	0.5 Typical @ +25°C				V
Max. (Peak) VOLP During Switching of Other Outputs (Output Under Test Not Switching)		VOLP See Figure 1	5	1 Typical @ +25°C				V
Input Capacitance		CI	-	-	10	-	10	pF
3-State Output Capacitance		CO	-	-	15	-	15	pF

†5V: min. is @ 5.5V
max. is @ 4.5V
5V: min. is @ 5.25V for 0°C to +70°C
max. is @ 4.75V for 0°C to +70°C

§CPD, measured per latch, is used to determine the dynamic power consumption.
PD (per package) = VCC ICC + Σ (VCC^2 fi CPD + VO^2 fo CL + VCC ΔICC D) where:
VCC = supply voltage
ΔICC = flow through current x unit load
CL = output load capacitance
D = duty cycle of input high
fo = output frequency
fi = input frequency

PARAMETER MEASUREMENT INFORMATION



NOTES:

1. VOLP is measured with respect to a ground reference near the output under test. VOHV is measured with respect to VOH.
2. Input pulses have the following characteristics: PRR ≤ 1MHz, tr = 2.5ns, tf = 2.5ns, skew 1ns.
3. R.F. fixture with 700-MHz design rules required. IC should be soldered into test board and bypassed with 0.1μF capacitor. Scope and probes require 700-MHz bandwidth.

Figure 1 - Simultaneous switching transient waveforms.

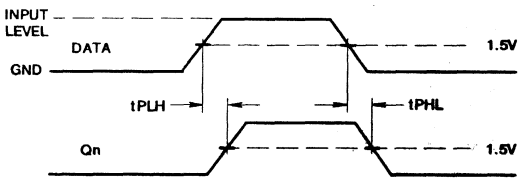


Figure 2 - Data to Qn propagation delays.

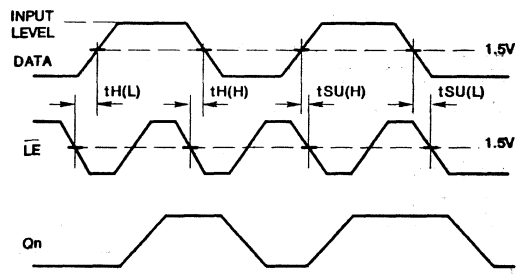
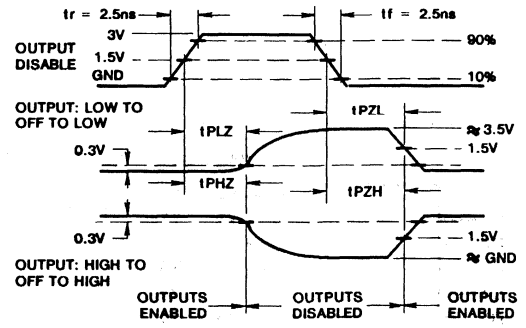
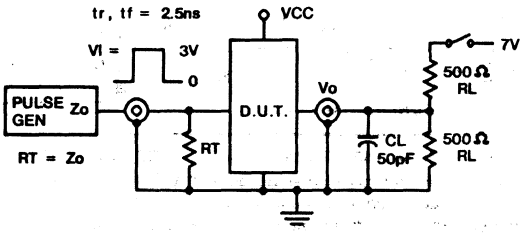


Figure 3 - Latch Enable prerequisite times.





TEST	SWITCH POSITION
tPLZ, tPZL, OPEN DRAIN	CLOSED
tPHZ, tPZH, tPLH, tPHL	OPEN

Figure 4 - Three-state propagation delay times and test circuit.

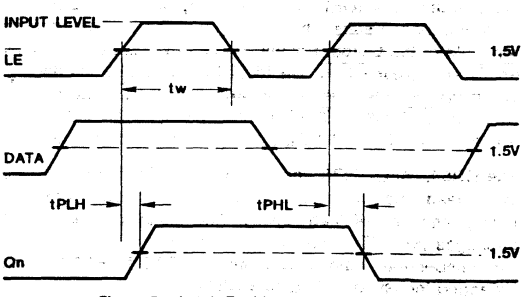
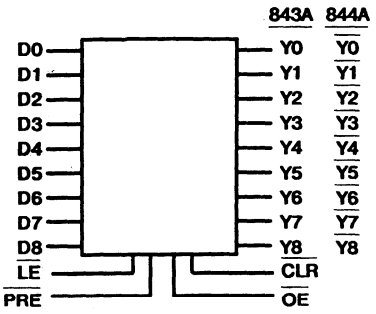


Figure 5 - Latch Enable propagation delays.

CD54/74FCT843A, CD54/74FCT844A



FUNCTIONAL DIAGRAM

9-Bit Transparent Latch, 3-State

CD54/74FCT843A - Non-Inverting
CD54/74FCT844A - Inverting

Type Features:

- *Buffered inputs*
- *Typical propagation delay: 3.5ns @ VCC = 5V, TA = +25°C, CL = 50pF*

The CD54/74FCT843A and CD54/74FCT844A transparent latches use a small-geometry BiMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output-HIGH level to two diode drops below VCC. This resultant lowering of output swing (0V to 3.7V) reduces power bus ringing (a source of EMI) and minimizes VCC bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 32 to 48 milliamperes.

The CD54/74FCT843A and CD54/74FCT844A outputs are transparent to the inputs when the Latch Enable ($\overline{LE}$) is HIGH. When the Latch Enable ($\overline{LE}$) goes LOW, the data is latched. The Output Enable ($\overline{OE}$) controls the 3-state outputs. When the Output Enable ($\overline{OE}$) is HIGH, the outputs outputs are in the high-impedance state. The latch operation is independent of the state of the Output Enable. These devices, having Preset ($\overline{PRE}$) and Clear ($\overline{CLR}$), are ideal for parity bus interfacing. When $\overline{PRE}$ is LOW, the outputs are HIGH if $\overline{OE}$ is LOW. $\overline{PRE}$ overrides $\overline{CLR}$. When $\overline{CLR}$ is LOW, the outputs are LOW if $\overline{OE}$ is LOW. When $\overline{CLR}$ is HIGH, data can be entered into the latch.

The CD54/74FCT843A and CD54/74FCT844A are supplied in 24-lead dual-in-line narrow-body plastic packages (EN suffix) and in 24-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over two temperature ranges: Commercial (0°C to +70°C) and Extended Industrial (-55°C to +125°C).

The CD54FCT843A and CD54FCT844A are also available in chip form (H suffix). These unpackaged devices are operable over the -55°C to +125°C temperature range.

Family Features:

- *SCR-latchup-resistant CMOS process and circuit design*
- *Speed of bipolar FAST*/AS/S with significantly reduced power consumption*
- *48/32-mA output sink current (commercial/extended industrial)*
- *Output voltage swing limited to 3.7V @ VCC = 5V*
- *Controlled output-edge rates*
- *Input/output isolation to VCC*
- *BiMOS technology with low quiescent power*

* FAST is a registered trademark of Fairchild Semiconductor Corp.

FUNCTION TABLES

INPUTS						OUTPUTS	
$\overline{CLR}$	$\overline{PRE}$	$\overline{OE}$	$\overline{LE}$	843A Dn	844A Dn	Yn	FUNCTION
H	H	H	X	X	X	Z	High Z
H	H	H	L	X	X	Z	Latched (High Z)
H	H	L	H	L	H	L	Transparent
H	H	L	H	H	L	H	Transparent
H	H	L	L	X	X	NC	Latched
H	L	L	X	X	X	H	Preset
L	H	L	X	X	X	L	Clear
L	L	L	X	X	X	H	Preset
L	H	H	L	X	X	Z	Latched (High Z)
H	L	H	L	X	X	Z	Latched (High Z)

H = HIGH, L = LOW, X = Immaterial,
NC = No Change, Z = High Impedance

Printed in USA/8-89

File Number **2396**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (VCC) ..... -0.5V to 6V
DC INPUT DIODE CURRENT, IIK (for VI < -0.5V) ..... -20mA
DC OUTPUT DIODE CURRENT, IOK (for VO < -0.5V) ..... -50mA
DC OUTPUT SINK CURRENT per Output Pin, IO ..... +70mA
DC OUTPUT SOURCE CURRENT per Output Pin, IO ..... -30mA
DC VCC CURRENT (ICC) 237mA
DC GROUND CURRENT (IGND) 453mA
POWER DISSIPATION PER PACKAGE (PD):
For TA = -55°C to +100°C (PACKAGE TYPE E) 500mW
For TA = +100°C to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8mW/°C to 300mW
For TA = -55°C to +70°C (PACKAGE TYPE M) 400mW
For TA = +70°C to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6mW/°C to 70mW
OPERATING-TEMPERATURE RANGE (TA):
PACKAGE TYPE E, M ..... -55°C to +125°C
STORAGE TEMPERATURE (Tstg) ..... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 in. ± 1/32 in. (1.59mm ± 0.79mm) from case for 10s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59mm) with solder contacting lead tips only ..... +300°C

RECOMMENDED OPERATING CONDITIONS:

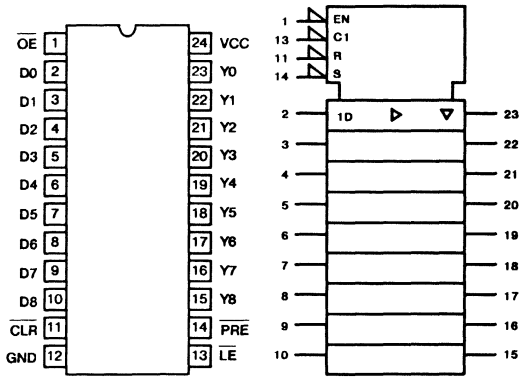
The following are normal operating ranges for these devices. For maximum reliability, devices should always be operated within these ranges.

CHARACTERISTIC		LIMITS MIN	LIMITS MAX	UNITS
Supply-Voltage Range, VCC*:	CD74 Series, TA = 0°C to 70°C	4.75	5.25	V
	CD54 Series, TA = -55°C to +125°C	4.5	5.5	V
DC Input Voltage, VI		0	VCC	V
DC Output Voltage, VO		0	≤VCC	V
Operating Temperature, TA		-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv		0	10	ns/V

* Unless otherwise specified, all voltages are referenced to ground.

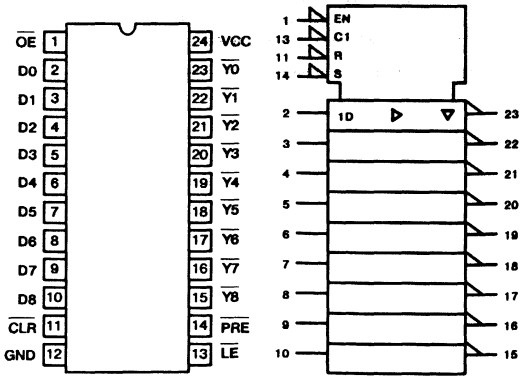
3

CD54/74FCT843A TYPES



TERMINAL ASSIGNMENT IEC LOGIC SYMBOL

CD54/74FCT844A TYPES



TERMINAL ASSIGNMENT IEC LOGIC SYMBOL

STATIC ELECTRICAL CHARACTERISTICS

FCT Series: 74FCT Commercial Temperature Range, 0°C to +70°C; VCC max = 5.25V, VCC min = 4.75V
54FCT Extended Industrial Temperature Range, -55°C to +125°C; VCC max = 5.5V, VCC min = 4.5V

CHARACTERISTICS		TEST CONDITIONS VI (V)	TEST CONDITIONS IO (mA)	VCC (V)	AMBIENT TEMPERATURE (TA) +25°C MIN	+25°C MAX	0°C to +70°C MIN	0°C to +70°C MAX	-55°C to +125°C MIN	-55°C to +125°C MAX	UNITS
High-Level Input Voltage	VIH			4.5 to 5.5	2	-	2	-	2	-	V
Low-Level Input Voltage	VIL			4.5 to 5.5	-	0.8	-	0.8	-	0.8	V
High-Level Output Voltage	VOH	VIH or	-24	MIN	2.4	-	2.4	-	-	-	V
		VIL	-20	MIN	2.4	-	-	-	2.4	-	V
Low-Level Output Voltage	VOL	VIH or	48	MIN	-	0.55	-	0.55	-	-	V
		VIL	32	MIN	-	0.55	-	-	-	0.55	V
High-Level Input Current	IIH	VCC		MAX	-	0.1	-	1	-	1	µA
Low-Level Input Current	IIL	GND		MAX	-	-0.1	-	-1	-	-1	µA
3-State Leakage Current	IOZH	VCC		MAX	-	0.5	-	10	-	10	µA
	IOZL	GND		MAX	-	-0.5	-	-10	-	-10	µA
Short-Circuit Output Current *	IOS	VCC or GND VO = 0		MAX	-60	-	-60	-	-60	-	mA
Input Clamp Voltage	VIK	VCC or GND	-18	MIN	-	-1.2	-	-1.2	-	-1.2	V
Quiescent Supply Current, MSI	ICC	VCC or GND	0	MAX	-	8	-	80	-	500	µA
Additional Quiescent Supply Current per Input Pin TTL Inputs High, 1 Unit Load	ΔICC	3.4V†		MAX	-	1.6	-	1.6	-	2	mA

* Not more than one output should be shorted at one time. Test duration should not exceed 100ms.
† Inputs that are not measured are at VCC or GND.

FCT Input Loading: All inputs are 1 unit load. Unit load is ΔICC limit specified in Static Characteristics Chart, e.g., 1.6mA max. @ +70°C.

PREREQUISITE FOR SWITCHING

CHARACTERISTICS		SYMBOL	VCC (V)	AMBIENT TEMPERATURE (TA) 0°C to +70°C MIN	0°C to +70°C MAX	-55°C to +125°C MIN	-55°C to +125°C MAX	UNITS
Pulse Width	$\overline{LE}$	tW	5†	6	–	6	–	ns
	$\overline{PRE}$, $\overline{CLR}$	tW	5	8	–	9	–	ns
Recovery Time	$\overline{PRE}$, $\overline{CLR}$	tREC	5	14	–	17	–	ns
Setup Time	Data to $\overline{LE}$	tSU	5	2.5	–	2.5	–	ns
Hold Time	Data to $\overline{LE}$	tH	5	2.5	–	3	–	ns

†5V: min. is @ 4.5V
5V: min. is @ 4.75V for 0°C to +70°C

SWITCHING CHARACTERISTICS

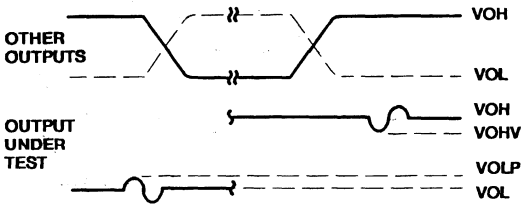
FCT Series: tr, tf = 2.5ns, CL = 50pF, RL - See Figure 4

CHARACTERISTICS		SYMBOL	VCC (V)	AMBIENT TEMPERATURE (TA) 0°C to +70°C MIN	0°C to +70°C MAX	-55°C to +125°C MIN	-55°C to +125°C MAX	UNITS
Propagation Delays: Data to Outputs	FCT843A	tPLH, tPHL	5†	1.5	9.5	1.5	11	ns
	FCT844A	tPLH, tPHL	5	1.5	10	1.5	12	ns
$\overline{LE}$ to Outputs		tPLH, tPHL	5	1.5	12	1.5	16	ns
$\overline{PRE}$ to Outputs		tPLH	5	1.5	12	1.5	14	ns
$\overline{CLR}$ to Outputs		tPHL	5	1.5	13	1.5	15	ns
Output Enable Times		tPZL, tPZH	5	1.5	14	1.5	15	ns
Output Disable Times		tPLZ, tPHZ	–	1.5	12	1.5	12	ns
Power Dissipation Capacitance	FCT843A	CPD§	–					pF
	FCT844A	CPD§	–					pF
Min. (Valley) VOHV During Switching of Other Outputs (Output Under Test Not Switching)		VOHV See Figure 1	5	0.5 Typical @ +25°C				V
Max. (Peak) VOLP During Switching of Other Outputs (Output Under Test Not Switching)		VOLP See Figure 1	5	1 Typical @ +25°C				V
Input Capacitance		CI	–	–	10	–	10	pF
3-State Output Capacitance		CO	–	–	15	–	15	pF

†5V: min. is @ 5.5V
max. is @ 4.5V
5V: min. is @ 5.25V for 0°C to +70°C
max. is @ 4.75V for 0°C to +70°C

§CPD, measured per latch, is used to determine the dynamic power consumption.
PD (per package) = VCC ICC + Σ (VCC² fi CPD + VO² fo CL + VCC ΔICC D) where:
VCC = supply voltage
ΔICC = flow through current x unit load
CL = output load capacitance
D = duty cycle of input high
fo = output frequency
fi = input frequency

PARAMETER MEASUREMENT INFORMATION



NOTES:

1. VOLP is measured with respect to a ground reference near the output under test. VOHV is measured with respect to VOH.
2. Input pulses have the following characteristics: PRR ≤ 1MHz, tr = 2.5ns, tf = 2.5ns, skew 1ns.
3. R.F. fixture with 700-MHz design rules required. IC should be soldered into test board and bypassed with 0.1µF capacitor. Scope and probes require 700-MHz bandwidth.

Figure 1 - Simultaneous switching transient waveforms.

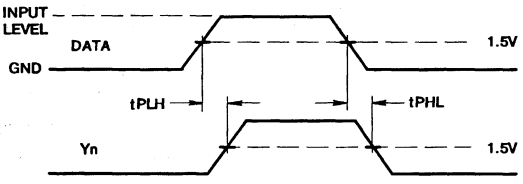


Figure 2 - Data to Yn propagation delays.

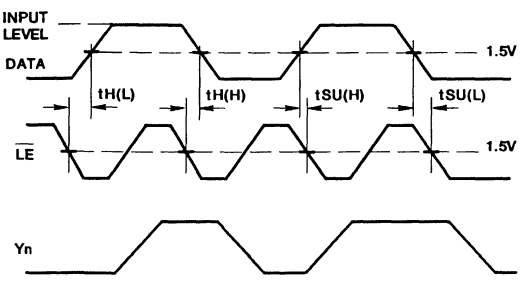
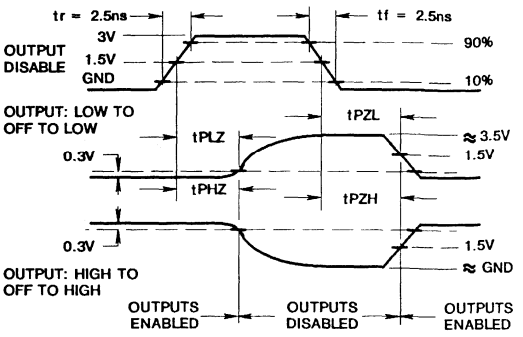
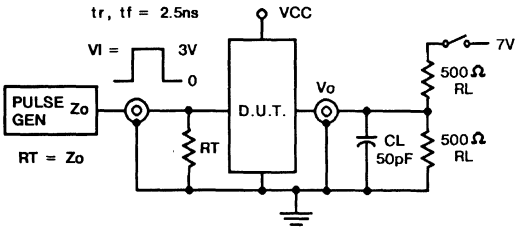


Figure 3 - Latch Enable prerequisite times.





TEST	SWITCH POSITION
tPLZ, tPZL, OPEN DRAIN	CLOSED
tPHZ, tPZH, tPLH, tPHL	OPEN

Figure 4 - Three-state propagation delay times and test circuit.

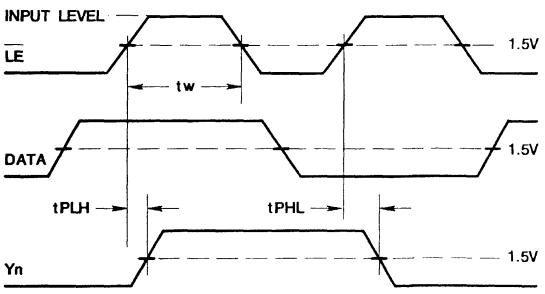
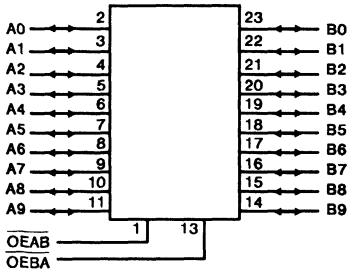


Figure 5 - Latch Enable propagation delays.

CD54/74FCT861A, CD54/74FCT862A



CD54/74FCT861A FUNCTIONAL DIAGRAM

10-Bit Bus Transceivers, 3-State

CD54/74FCT861A - Non-Inverting
CD54/74FCT862A - Inverting

Type Features:

- *Buffered inputs*
- *Typical propagation delay: 3ns @ VCC = 5V, TA = 25°C, CL = 50pF*

Family Features:

- *SCR-latchup-resistant CMOS process and circuit design*
- *Speed of bipolar FAST*/AS/S with significantly reduced power consumption*
- *48/32-mA output sink current (commercial/extended industrial)*
- *Output voltage swing limited to 3.7V @ VCC = 5V*
- *Controlled output-edge rates*
- *Input/output isolation to VCC*
- *BiMOS technology with low quiescent power*

* FAST is a registered trademark of Fairchild Semiconductor Corp.

The CD54/74FCT861A and CD54/74FCT862A 10-bit bus transceivers use a small-geometry BiMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output-HIGH level to two diode drops below VCC. This resultant lowering of output swing (0V to 3.7V) reduces power bus ringing (a source of EMI) and minimizes VCC bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 32 to 48 milliamperes.

These devices provide extra data width for wider address/data paths or buses carrying parity. The dual Output Enable provision gives these devices the capability to store data by simultaneously enabling $\overline{OEAB}$ and $\overline{OEBA}$. Each output reinforces its input under these conditions, and when all other data sources to the bus lines are at high impedance, both sets of bus lines will remain in their last states.

The CD54/74FCT861A and CD54/74FCT862A are supplied in 24-lead dual-in-line narrow-body plastic packages (EN suffix) and in 24-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over two temperature ranges: Commercial (0°C to +70°C) and Extended Industrial (-55°C to +125°C).

The CD54FCT861A and CD54FCT862A are also available in-chip form (H suffix). These unpackaged devices are operable over the -55°C to +125°C temperature range.

FUNCTION TABLES

CD54/74FCT861A (NON-INVERTING)

INPUTS				OUTPUTS		
$\overline{OEBA}$	$\overline{OEAB}$	B	A	B	A	FUNCTION
L	H	L	N/A	N/A	L	B Data to A Bus
L	H	H	N/A	N/A	H	B Data to A Bus
H	L	N/A	L	L	N/A	A Data to B Bus
H	L	N/A	H	H	N/A	A Data to B Bus
H	H	X	X	Z	Z	High Z
L	L	-	-	-	-	A Data to B Bus, B Data to A Bus

CD54/74FCT862A (INVERTING)

INPUTS				OUTPUTS		
$\overline{OEBA}$	$\overline{OEAB}$	$\overline{B}$	$\overline{A}$	$\overline{B}$	$\overline{A}$	FUNCTION
L	H	L	N/A	N/A	H	B Data to A Bus
L	H	H	N/A	N/A	L	B Data to A Bus
H	L	N/A	L	H	N/A	A Data to B Bus
H	L	N/A	H	L	N/A	A Data to B Bus
H	H	X	X	Z	Z	High Z
L	L	-	-	-	-	A Data to B Bus, B Data to A Bus

H = HIGH, L = LOW, Z = HIGH Impedance, X = Immaterial, N/A = Not Applicable

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File Number 2392

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (VCC) ..... -0.5V to 6V
DC INPUT DIODE CURRENT, IIK (for VI < -0.5V) ..... -20mA
DC OUTPUT DIODE CURRENT, IOK (for VO < -0.5V) ..... -50mA
DC OUTPUT SINK CURRENT per Output Pin, IO ..... +70mA
DC OUTPUT SOURCE CURRENT per Output Pin, IO ..... -30mA
DC VCC CURRENT (ICC) 264mA
DC GROUND CURRENT (IGND) 500mA
POWER DISSIPATION PER PACKAGE (PD):
For TA = -55°C to +100°C (PACKAGE TYPE E) 500mW
For TA = +100°C to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8mW/°C to 300mW
For TA = -55°C to +70°C (PACKAGE TYPE M) 400mW
For TA = +70°C to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6mW/°C to 70mW
OPERATING-TEMPERATURE RANGE (TA):
PACKAGE TYPE E, M ..... -55°C to +125°C
STORAGE TEMPERATURE (Tstg) ..... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 in. ± 1/32 in. (1.59mm ± 0.79mm) from case for 10s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59mm) with solder contacting lead tips only ..... +300°C

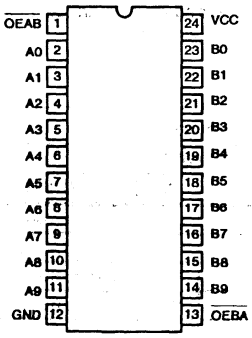
RECOMMENDED OPERATING CONDITIONS:

The following are normal operating ranges for these devices. For maximum reliability, devices should always be operated within these ranges.

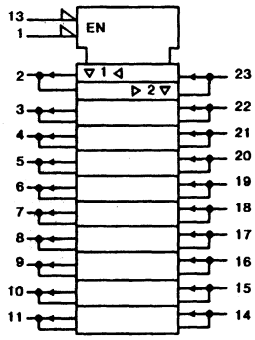
CHARACTERISTIC		LIMITS MIN	LIMITS MAX	UNITS
Supply-Voltage Range, VCC*:	CD74 Series, TA = 0°C to 70°C	4.75	5.25	V
	CD54 Series, TA = -55°C to +125°C	4.5	5.5	V
DC Input Voltage, VI		0	VCC	V
DC Output Voltage, VO		0	≤ VCC	V
Operating Temperature, TA		-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv		0	10	ns/V

* Unless otherwise specified, all voltages are referenced to ground.

CD54/74FCT861A TYPES

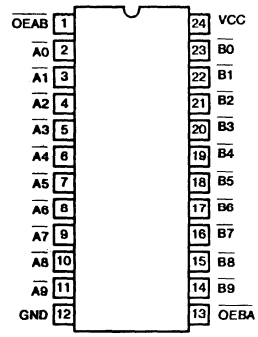


TERMINAL ASSIGNMENT

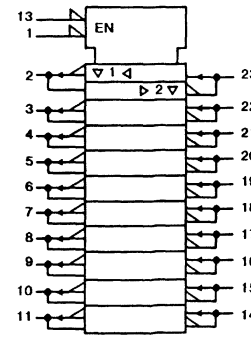


IEC LOGIC SYMBOL

CD54/74FCT862A TYPES



TERMINAL ASSIGNMENT



IEC LOGIC SYMBOL

STATIC ELECTRICAL CHARACTERISTICS

FCT Series: 74FCT Commercial Temperature Range, 0°C to +70°C; VCC max = 5.25V, VCC min = 4.75V
54FCT Extended Industrial Temperature Range, -55°C to +125°C; VCC max = 5.5V, VCC min = 4.5V

CHARACTERISTICS		TEST CONDITIONS VI (V)	TEST CONDITIONS IO (mA)	VCC (V)	AMBIENT TEMPERATURE (TA) +25°C MIN	+25°C MAX	0°C to +70°C MIN	0°C to +70°C MAX	-55°C to +125°C MIN	-55°C to +125°C MAX	UNITS
High-Level Input Voltage	VIH			4.5 to 5.5	2	-	2	-	2	-	V
Low-Level Input Voltage	VIL			4.5 to 5.5	-	0.8	-	0.8	-	0.8	V
High-Level Output Voltage	VOH	VIH or	-24	MIN	2.4	-	2.4	-	-	-	V
		VIL	-20	MIN	2.4	-	-	-	2.4	-	V
Low-Level Output Voltage	VOL	VIH or	48	MIN	-	0.55	-	0.55	-	-	V
		VIL	32	MIN	-	0.55	-	-	-	0.55	V
High-Level Input Current	IIH	VCC		MAX	-	0.1	-	1	-	1	µA
Low-Level Input Current	IIL	GND		MAX	-	-0.1	-	-1	-	-1	µA
3-State Leakage Current	IOZH	VCC		MAX	-	0.5	-	10	-	10	µA
	IOZL	GND		MAX	-	-0.5	-	-10	-	-10	µA
Short-Circuit Output Current *	IOS	VCC or GND VO = 0		MAX	-60	-	-60	-	-60	-	mA
Input Clamp Voltage	VIK	VCC or GND	-18	MIN	-	-1.2	-	-1.2	-	-1.2	V
Quiescent Supply Current, MSI	ICC	VCC or GND	0	MAX	-	8	-	80	-	500	µA
Additional Quiescent Supply Current per Input Pin TTL Inputs High, 1 Unit Load	ΔICC	3.4V†		MAX	-	1.6	-	1.6	-	2	mA

* Not more than one output should be shorted at one time. Test duration should not exceed 100ms.
† Inputs that are not measured are at VCC or GND.

FCT Input Loading: All inputs are 1 unit load. Unit load is ΔICC limit specified in Static Characteristics Chart, e.g., 1.6mA max. @ +70°C.

3

SWITCHING CHARACTERISTICS

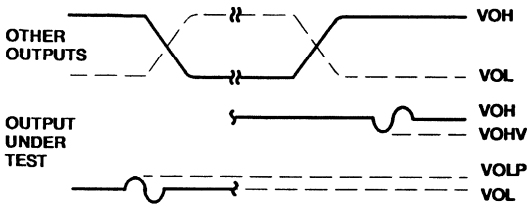
FCT Series: tr, tf = 2.5ns, CL = 50pF, RL - See Figure 3

CHARACTERISTICS		SYMBOL	VCC (V)	AMBIENT TEMPERATURE (TA) 0°C to +70°C MIN	0°C to +70°C MAX	-55°C to +125°C MIN	-55°C to +125°C MAX	UNITS
Propagation Delays: Data to Outputs	FCT861A	tPLH, tPHL	5†	1.5	8	1.5	10	ns
	FCT862A	tPLH, tPHL	5	1.5	7.5	1.5	9.5	ns
Output Disable to Output		tPLZ, tPHZ	5	1.5	17	1.5	19	ns
Output Enable to Output		tPZH, tPZL	5	1.5	15	1.5	17	ns
Power Dissipation Capacitance		CPD§	-					pF
Min. (Valley) VOHV During Switching of Other Outputs (Output Under Test Not Switching)		VOHV See Figure 1	5	0.5 Typical @ +25°C				V
Max. (Peak) VOLP During Switching of Other Outputs (Output Under Test Not Switching)		VOLP See Figure 1	5	1 Typical @ +25°C				V
Input Capacitance		CI	-	-	10	-	10	pF
3-State Output Capacitance		CO	-	-	15	-	15	pF

†5V: min. is @ 5.5V
max. is @ 4.5V
5V: min. is @ 5.25V for 0°C to +70°C
max. is @ 4.75V for 0°C to +70°C

§CPD, measured per function, is used to determine the dynamic power consumption.
PD (per package) = VCC ICC + Σ (VCC^2 fi CPD + VO^2 fo CL + VCC ΔICC D) where:
VCC = supply voltage
ΔICC = flow through current x unit load
CL = output load capacitance
D = duty cycle of input high
fo = output frequency
fi = input frequency

PARAMETER MEASUREMENT INFORMATION



NOTES:
1. VOLP is measured with respect to a ground reference near the output under test. VOHV is measured with respect to VOH.
2. Input pulses have the following characteristics: PRR $\leq$ 1MHz, tr = 2.5ns, tf = 2.5ns, skew 1ns.
3. R.F. fixture with 700-MHz design rules required. IC should be soldered into test board and bypassed with 0.1µF capacitor. Scope and probes require 700-MHz bandwidth.

Figure 1 - Simultaneous switching transient waveforms.

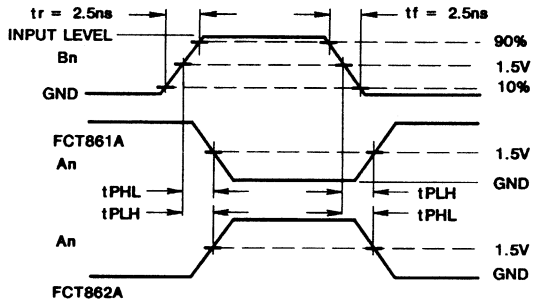
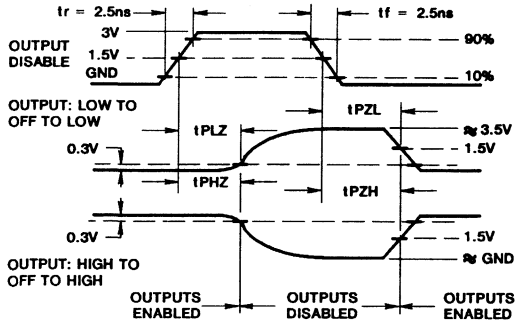
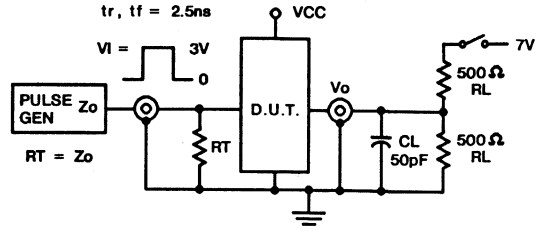


Figure 2 - Propagation delay times.

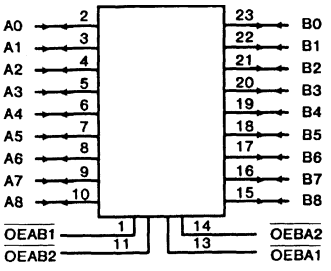




TEST	SWITCH POSITION
tPLZ, tPZL, OPEN DRAIN	CLOSED
tPHZ, tPZH, tPLH, tPHL	OPEN

Figure 3 - Three-state propagation delay times and test circuit.

CD54/74FCT863A, CD54/74FCT864A



CD54/74FCT863A
FUNCTIONAL DIAGRAM

9-Bit Bus Transceivers, 3-State

CD54/74FCT863A - Non-Inverting
CD54/74FCT864A - Inverting

Type Features:

- *Buffered inputs*
- *Typical propagation delay: 3ns @ VCC = 5V, TA = 25°C, CL = 50pF*

Family Features:

- *SCR-latchup-resistant CMOS process and circuit design*
- *Speed of bipolar FAST*/AS/S with significantly reduced power consumption*
- *48/32-mA output sink current (commercial/extended industrial)*
- *Output voltage swing limited to 3.7V @ VCC = 5V*
- *Controlled output-edge rates*
- *Input/output isolation to VCC*
- *BiMOS technology with low quiescent power*

* FAST is a registered trademark of Fairchild Semiconductor Corp.

The CD54/74FCT863A and CD54/74FCT864A 9-bit bus transceivers use a small-geometry BiMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output-HIGH level to two diode drops below VCC. This resultant lowering of output swing (0V to 3.7V) reduces power bus ringing (a source of EMI) and minimizes VCC bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 32 to 48 milliamperes.

These devices provide extra data width for wider address/data paths or buses carrying parity. They have NORed output enables for maximum control flexibility. The dual Output Enable provision gives these devices the capability to store data by simultaneously enabling $\overline{OEAB}$ and $\overline{OEBA}$. Each output reinforces its input under these conditions, and when all other data sources to the bus lines are at high impedance, both sets of bus lines will remain in their last states.

The CD54/74FCT863A and CD54/74FCT864A are supplied in 24-lead dual-in-line narrow-body plastic packages (EN suffix) and in 24-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over two temperature ranges: Commercial (0°C to +70°C) and Extended Industrial (-55°C to +125°C).

The CD54FCT863A and CD54FCT864A are also available in chip form (H suffix). These unpackaged devices are operable over the -55°C to +125°C temperature range.

FUNCTION TABLES

CD54/74FCT863A (NON-INVERTING)						
INPUTS				OUTPUTS		
$\overline{OEBA}$	$\overline{OEAB}$	B	A	B	A	FUNCTION
L	H	L	N/A	N/A	L	B Data to A Bus
L	H	H	N/A	N/A	H	B Data to A Bus
H	L	N/A	L	L	N/A	A Data to B Bus
H	L	N/A	H	H	N/A	A Data to B Bus
H	H	X	X	Z	Z	High Z
L	L	-	-	-	-	A Data to B Bus, B Data to A Bus

CD54/74FCT864A (INVERTING)						
INPUTS				OUTPUTS		
$\overline{OEBA}$	$\overline{OEAB}$	$\overline{B}$	$\overline{A}$	$\overline{B}$	$\overline{A}$	FUNCTION
L	H	L	N/A	N/A	H	B Data to A Bus
L	H	H	N/A	N/A	L	B Data to A Bus
H	L	N/A	L	H	N/A	A Data to B Bus
H	L	N/A	H	L	N/A	A Data to B Bus
H	H	X	X	Z	Z	High Z
L	L	-	-	-	-	A Data to B Bus, B Data to A Bus

H = HIGH, L = LOW, Z = HIGH Impedance, X = Immaterial, N/A = Not Applicable

Printed in USA/8-89

File Number **2391**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (VCC) ..... -0.5V to 6V
DC INPUT DIODE CURRENT, IIK (for VI < -0.5V) ..... -20mA
DC OUTPUT DIODE CURRENT, IOK (for VO < -0.5V) ..... -50mA
DC OUTPUT SINK CURRENT per Output Pin, IO ..... +70mA
DC OUTPUT SOURCE CURRENT per Output Pin, IO ..... -30mA
DC VCC CURRENT (ICC) 234mA
DC GROUND CURRENT (IGND) 455mA
POWER DISSIPATION PER PACKAGE (PD):
For TA = -55°C to +100°C (PACKAGE TYPE E) 500mW
For TA = +100°C to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8mW/°C to 300mW
For TA = -55°C to +70°C (PACKAGE TYPE M) 400mW
For TA = +70°C to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6mW/°C to 70mW
OPERATING-TEMPERATURE RANGE (TA):
PACKAGE TYPE E, M ..... -55°C to +125°C
STORAGE TEMPERATURE (Tstg) ..... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 in. ± 1/32 in. (1.59mm ± 0.79mm) from case for 10s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59mm) with solder contacting lead tips only ..... +300°C

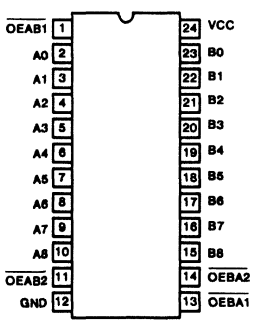
RECOMMENDED OPERATING CONDITIONS:

The following are normal operating ranges for these devices. For maximum reliability, devices should always be operated within these ranges.

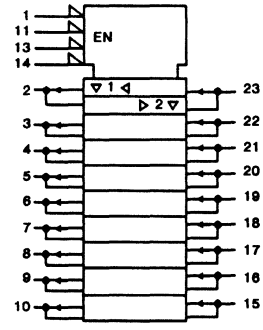
CHARACTERISTIC		LIMITS MIN	LIMITS MAX	UNITS
Supply-Voltage Range, VCC*:	CD74 Series, TA = 0°C to 70°C	4.75	5.25	V
	CD54 Series, TA = -55°C to +125°C	4.5	5.5	V
DC Input Voltage, VI		0	VCC	V
DC Output Voltage, VO		0	≤ VCC	V
Operating Temperature, TA		-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv		0	10	ns/V

* Unless otherwise specified, all voltages are referenced to ground.

CD54/74FCT863A TYPES

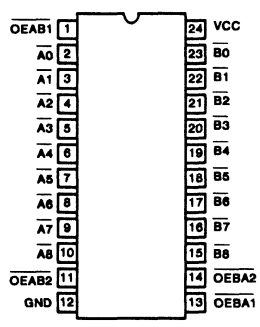


TERMINAL ASSIGNMENT



IEC LOGIC SYMBOL

CD54/74FCT864A TYPES



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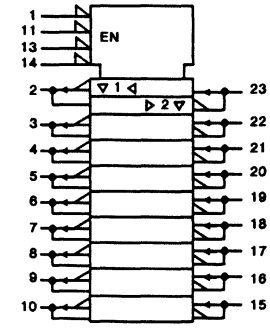


IEC LOGIC SYMBOL

STATIC ELECTRICAL CHARACTERISTICS

FCT Series: 74FCT Commercial Temperature Range, 0°C to +70°C; VCC max = 5.25V, VCC min = 4.75V
54FCT Extended Industrial Temperature Range, -55°C to +125°C; VCC max = 5.5V, VCC min = 4.5V

CHARACTERISTICS		TEST CONDITIONS			AMBIENT TEMPERATURE (TA)						UNITS
					+25°C		0°C to +70°C		-55°C to +125°C		
		VI (V)	IO (mA)	VCC (V)	MIN	MAX	MIN	MAX	MIN	MAX	
High-Level Input Voltage	VIH			4.5 to 5.5	2	-	2	-	2	-	V
Low-Level Input Voltage	VIL			4.5 to 5.5	-	0.8	-	0.8	-	0.8	V
High-Level Output Voltage	VOH	VIH or	-24	MIN	2.4	-	2.4	-	-	-	V
		VIL	-20	MIN	2.4	-	-	-	2.4	-	V
Low-Level Output Voltage	VOL	VIH or	48	MIN	-	0.55	-	0.55	-	-	V
		VIL	32	MIN	-	0.55	-	-	-	0.55	V
High-Level Input Current	IIH	VCC		MAX	-	0.1	-	1	-	1	µA
Low-Level Input Current	IIL	GND		MAX	-	-0.1	-	-1	-	-1	µA
3-State Leakage Current	IOZH	VCC		MAX	-	0.5	-	10	-	10	µA
	IOZL	GND		MAX	-	-0.5	-	-10	-	-10	µA
Short-Circuit Output Current *	IOS	VCC or GND VO = 0		MAX	-60	-	-60	-	-60	-	mA
Input Clamp Voltage	VIK	VCC or GND	-18	MIN	-	-1.2	-	-1.2	-	-1.2	V
Quiescent Supply Current, MSI	ICC	VCC or GND	0	MAX	-	8	-	80	-	500	µA
Additional Quiescent Supply Current per Input Pin TTL Inputs High, 1 Unit Load	ΔICC	3.4V†		MAX	-	1.6	-	1.6	-	2	mA

* Not more than one output should be shorted at one time. Test duration should not exceed 100ms.
† Inputs that are not measured are at VCC or GND.

FCT Input Loading: All inputs are 1 unit load. Unit load is ΔICC limit specified in Static Characteristics Chart, e.g., 1.6mA max. @ +70°C.

SWITCHING CHARACTERISTICS

FCT Series: tr, tf = 2.5ns, CL = 50pF, RL - See Figure 3

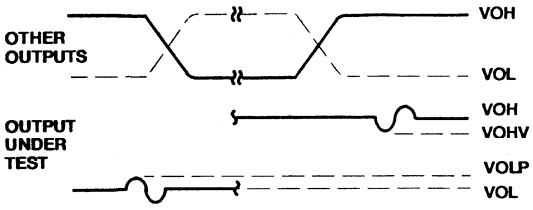
CHARACTERISTICS		SYMBOL	VCC (V)	AMBIENT TEMPERATURE (TA) 0°C to +70°C MIN	0°C to +70°C MAX	-55°C to +125°C MIN	-55°C to +125°C MAX	UNITS
Propagation Delays: Data to Outputs	FCT863A	tPLH, tPHL	5†	1.5	8	1.5	10	ns
	FCT864A	tPLH, tPHL	5	1.5	7.5	1.5	9.5	ns
Output Disable to Output		tPLZ, tPHZ	5	1.5	17	1.5	19	ns
Output Enable to Output		tPZH, tPZL	5	1.5	15	1.5	17	ns
Power Dissipation Capacitance		CPD§	-					pF
Min. (Valley) VOHV During Switching of Other Outputs (Output Under Test Not Switching)		VOHV See Figure 1	5	0.5 Typical @ +25°C				V
Max. (Peak) VOLP During Switching of Other Outputs (Output Under Test Not Switching)		VOLP See Figure 1	5	1 Typical @ +25°C				V
Input Capacitance		CI	-	-	10	-	10	pF
3-State Output Capacitance		CO	-	-	15	-	15	pF

†5V: min. is @ 5.5V
max. is @ 4.5V
5V: min. is @ 5.25V for 0°C to +70°C
max. is @ 4.75V for 0°C to +70°C

§CPD, measured per function, is used to determine the dynamic power consumption.
PD (per package) = VCC ICC + Σ (VCC^2 fi CPD + VO^2 fo CL + VCC ΔICC D) where:
VCC = supply voltage
ΔICC = flow through current x unit load
CL = output load capacitance
D = duty cycle of input high
fo = output frequency
fi = input frequency

3

PARAMETER MEASUREMENT INFORMATION



NOTES:

1. VOLP is measured with respect to a ground reference near the output under test. VOHV is measured with respect to VOH.
2. Input pulses have the following characteristics: PRR ≤ 1MHz, tr = 2.5ns, tf = 2.5ns, skew 1ns.
3. R.F. fixture with 700-MHz design rules required. IC should be soldered into test board and bypassed with 0.1μF capacitor. Scope and probes require 700-MHz bandwidth.

Figure 1 - Simultaneous switching transient waveforms.

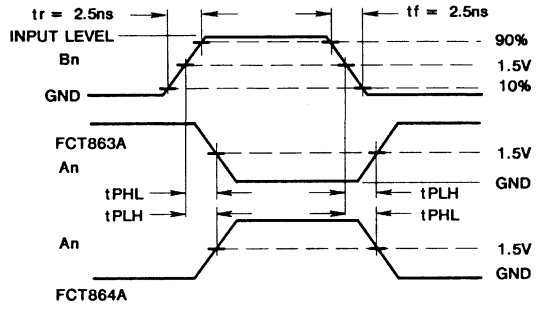
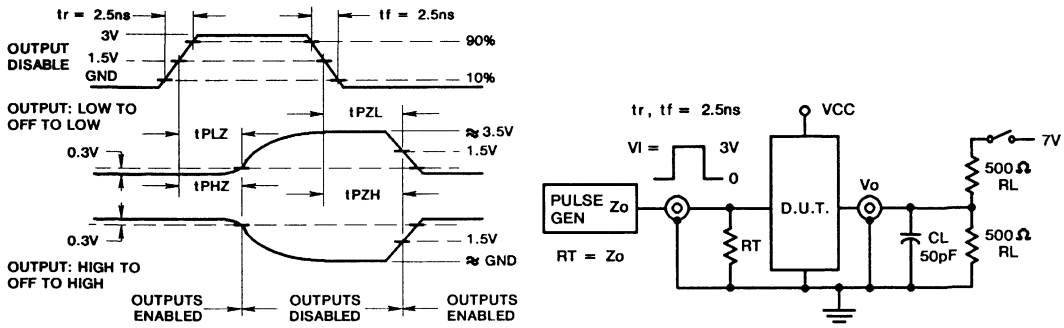


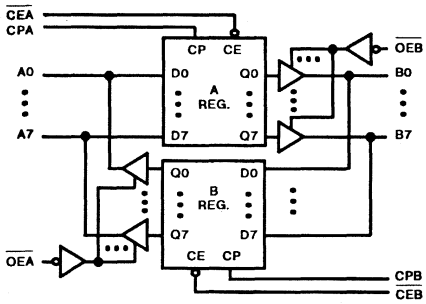
Figure 2 - Propagation delay times.



TEST	SWITCH POSITION
tPLZ, tPZL, OPEN DRAIN	CLOSED
tPHZ, tPZH, tPLH, tPHL	OPEN

Figure 3 - Three-state propagation delay times and test circuit.

CD54/74FCT2952A, CD54/74FCT2953A



FUNCTIONAL DIAGRAM

Octal Register-Transceivers, 3-State

CD54/74FCT2952A - Non-Inverting
CD54/74FCT2953A - Inverting

Type Features:

- *Buffered inputs*
- *Typical propagation delay: 3.5ns @ VCC = 5V, TA = 25°C, CL = 50pF*

3

The CD54/74FCT2952A and CD54/74FCT2953A octal register-transceivers use a small-geometry BiMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output-HIGH level to two diode drops below VCC. This resultant lowering of output swing (0V to 3.7V) reduces power bus ringing (a source of EMI) and minimizes VCC bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 48 to 64 milliamperes.

These devices contain two 8-bit back-to-back registers that store data flowing in both directions between two bidirectional buses. Each register has separate clock, clock enable, and 3-state output enable signals associated with it.

The CD54/74FCT2952A and CD54/74FCT2953A are supplied in 24-lead dual-in-line narrow-body plastic packages (EN suffix) and in 24-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over two temperature ranges: Commercial (0°C to +70°C) and Extended Industrial (-55°C to +125°C).

Family Features:

- *SCR-latchup-resistant CMOS process and circuit design*
- *Speed of bipolar FAST*/AS/S with significantly reduced power consumption*
- *64/48-mA output sink current (commercial/extended industrial)*
- *Output voltage swing limited to 3.7V @ VCC = 5V*
- *Controlled output-edge rates*
- *Input/output isolation to VCC*
- *BiMOS technology with low quiescent power*

* FAST is a registered trademark of Fairchild Semiconductor Corp.

The CD54FCT2952A and CD54FCT2953A are also available in chip form (H suffix). These unpackaged devices are operable over the -55°C to +125°C temperature range.

REGISTER FUNCTION TABLE (APPLIES TO A OR B REGISTER)

INPUTS			INTERNAL	
D	CP	$\overline{CE}$	Q	FUNCTION
X	X	H	NC	Hold Data
L	⎍	L	L	Load Data
H	⎍	L	H	

OUTPUT CONTROL

	INTERNAL	OUTPUTS		
$\overline{OE}$	Q	FCT2952A	FCT2953A	FUNCTION
H	X	Z	Z	Disable Outputs
L	L	L	H	Enable Outputs
L	H	H	L	

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File Number **2400**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (VCC) ..... -0.5V to 6V
DC INPUT DIODE CURRENT, IIK (for VI < -0.5V) ..... -20mA
DC OUTPUT DIODE CURRENT, IOK (for VO < -0.5V) ..... -50mA
DC OUTPUT SINK CURRENT per Output Pin, IO ..... +70mA
DC OUTPUT SOURCE CURRENT per Output Pin, IO ..... -30mA
DC VCC CURRENT (ICC) 140mA
DC GROUND CURRENT (IGND) 528mA
POWER DISSIPATION PER PACKAGE (PD):
For TA = -55°C to +100°C (PACKAGE TYPE E) 500mW
For TA = +100°C to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8mW/°C to 300mW
For TA = -55°C to +70°C (PACKAGE TYPE M) 400mW
For TA = +70°C to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6mW/°C to 70mW
OPERATING-TEMPERATURE RANGE (TA):
PACKAGE TYPE E, M ..... -55°C to +125°C
STORAGE TEMPERATURE (Tstg) ..... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 in. ± 1/32 in. (1.59mm ± 0.79mm) from case for 10s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59mm) with solder contacting lead tips only ..... +300°C

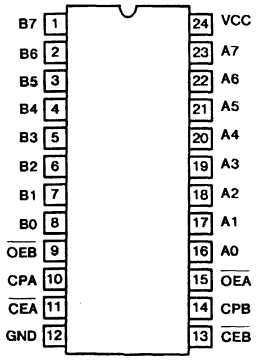
RECOMMENDED OPERATING CONDITIONS:

The following are normal operating ranges for these devices. For maximum reliability, devices should always be operated within these ranges.

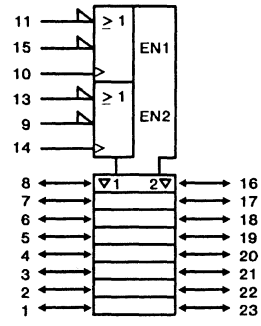
CHARACTERISTIC		LIMITS MIN	LIMITS MAX	UNITS
Supply-Voltage Range, VCC*:	CD74 Series, TA = 0°C to 70°C	4.75	5.25	V
	CD54 Series, TA = -55°C to +125°C	4.5	5.5	V
DC Input Voltage, VI		0	VCC	V
DC Output Voltage, VO		0	≤ VCC	V
Operating Temperature, TA		-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv		0	10	ns/V

* Unless otherwise specified, all voltages are referenced to ground.

CD54/74FCT2952A TYPES

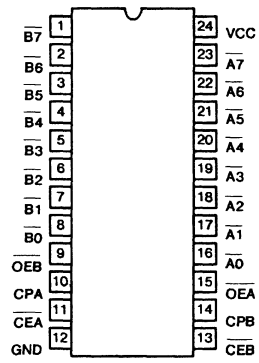


TERMINAL ASSIGNMENT



IEC LOGIC SYMBOL

CD54/74FCT2953A TYPES



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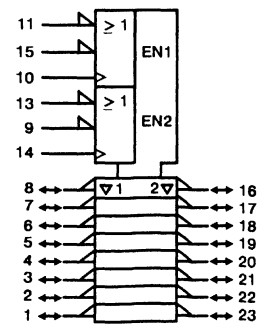


IEC LOGIC SYMBOL

STATIC ELECTRICAL CHARACTERISTICS

FCT Series: 74FCT Commercial Temperature Range, 0°C to +70°C; VCC max = 5.25V, VCC min = 4.75V
54FCT Extended Industrial Temperature Range, -55°C to +125°C; VCC max = 5.5V, VCC min = 4.5V

CHARACTERISTICS		TEST CONDITIONS VI (V)	TEST CONDITIONS IO (mA)	VCC (V)	AMBIENT TEMPERATURE (TA) +25°C MIN	+25°C MAX	0°C to +70°C MIN	0°C to +70°C MAX	-55°C to +125°C MIN	-55°C to +125°C MAX	UNITS
High-Level Input Voltage	VIH			4.5 to 5.5	2	-	2	-	2	-	V
Low-Level Input Voltage	VIL			4.5 to 5.5	-	0.8	-	0.8	-	0.8	V
High-Level Output Voltage	VOH	VIH or	-15	MIN	2.4	-	2.4	-	-	-	V
		VIL	-12	MIN	2.4	-	-	-	2.4	-	V
Low-Level Output Voltage	VOL	VIH or	64	MIN	-	0.55	-	0.55	-	-	V
		VIL	48	MIN	-	0.55	-	-	-	0.55	V
High-Level Input Current	IIH	VCC		MAX	-	0.1	-	1	-	1	µA
Low-Level Input Current	IIL	GND		MAX	-	-0.1	-	-1	-	-1	µA
3-State Leakage Current	IOZH	VCC		MAX	-	0.5	-	10	-	10	µA
	IOZL	GND		MAX	-	-0.5	-	-10	-	-10	µA
Short-Circuit Output Current *	IOS	VCC or GND VO = 0		MAX	-60	-	-60	-	-60	-	mA
Input Clamp Voltage	VIK	VCC or GND	-18	MIN	-	-1.2	-	-1.2	-	-1.2	V
Quiescent Supply Current, MSI	ICC	VCC or GND	0	MAX	-	8	-	80	-	500	µA
Additional Quiescent Supply Current per Input Pin TTL Inputs High, 1 Unit Load	ΔICC	3.4V†		MAX	-	1.6	-	1.6	-	2	mA

* Not more than one output should be shorted at one time. Test duration should not exceed 100ms.
† Inputs that are not measured are at VCC or GND.

FCT Input Loading: All inputs are 1 unit load. Unit load is ΔICC limit specified in Static Characteristics Chart, e.g., 1.6mA max. @ +70°C.

PREREQUISITE FOR SWITCHING

CHARACTERISTICS		SYMBOL	VCC (V)	AMBIENT TEMPERATURE (TA) 0°C to +70°C MIN	0°C to +70°C MAX	-55°C to +125°C MIN	-55°C to +125°C MAX	UNITS
Clock Pulse Width	CPA, CPB	tW	5†	3	-	3	-	ns
Setup Time	An, Bn to CPA, CPB	tSU	5	2	-	2.5	-	ns
	$\overline{CEA}$, $\overline{CEB}$ to CPA, CPB	tSU	5	2	-	2	-	ns
Hold Time	An, Bn to CPA, CPB	tH	5	2	-	2	-	ns
	$\overline{CEA}$, $\overline{CEB}$ to CPA, CPB	tH	5	2	-	2	-	ns

†5V: min. is @ 4.5V
5V: min. is @ 4.75V for 0°C to +70°C

SWITCHING CHARACTERISTICS

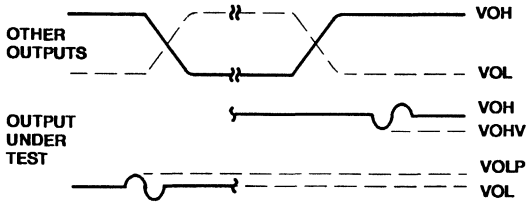
FCT Series: tr, tf = 2.5ns, CL = 50pF, RL - See Figure 4

CHARACTERISTICS		SYMBOL	VCC (V)	AMBIENT TEMPERATURE (TA) 0°C to +70°C MIN	0°C to +70°C MAX	-55°C to +125°C MIN	-55°C to +125°C MAX	UNITS
Propagation Delays:	CPA, CPB to Bn, An	tPLH, tPHL	5†	2	10	2	11	ns
Output Enable Time	$\overline{OEA}$ or $\overline{OEB}$ to An or Bn	tPZL, tPZH	5	1.5	10.5	1.5	13	ns
Output Disable Time	$\overline{OEA}$ or $\overline{OEB}$ to An or Bn	tPLZ, tPHZ	5	1.5	10	1.5	10	ns
Power Dissipation Capacitance		CPD§	-					pF
Min. (Valley) VOHV During Switching of Other Outputs (Output Under Test Not Switching)		VOHV See Figure 1	5	0.5 Typical @ +25°C				V
Max. (Peak) VOLP During Switching of Other Outputs (Output Under Test Not Switching)		VOLP See Figure 1	5	1 Typical @ +25°C				V
Input Capacitance		CI	-	-	10	-	10	pF
3-State Output Capacitance		CO	-	-	15	-	15	pF

†5V: min. is @ 5.5V
max. is @ 4.5V
5V: min. is @ 5.25V for 0°C to +70°C
max. is @ 4.75V for 0°C to +70°C

§CPD, measured per function, is used to determine the dynamic power consumption.
PD (per package) = VCC ICC + Σ (VCC^2 fi CPD + VO^2 fo CL + VCC ΔICC D) where:
VCC = supply voltage
ΔICC = flow through current x unit load
CL = output load capacitance
D = duty cycle of input high
fo = output frequency
fi = input frequency

PARAMETER MEASUREMENT INFORMATION



NOTES:

1. VOLP is measured with respect to a ground reference near the output under test. VOHV is measured with respect to VOH.
2. Input pulses have the following characteristics: PRR $\leq$ 1MHz, tr = 2.5ns, tf = 2.5ns, skew 1ns.
3. R.F. fixture with 700-MHz design rules required. IC should be soldered into test board and bypassed with 0.1µF capacitor. Scope and probes require 700-MHz bandwidth.

Figure 1 - Simultaneous switching transient waveforms.

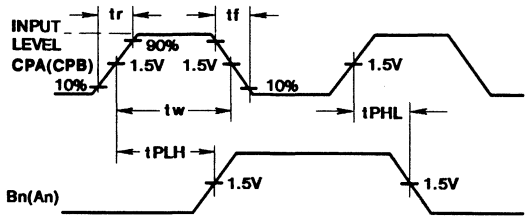


Figure 2 - CD54/74FCT2952A propagation delay times.

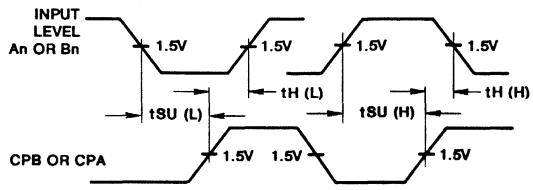
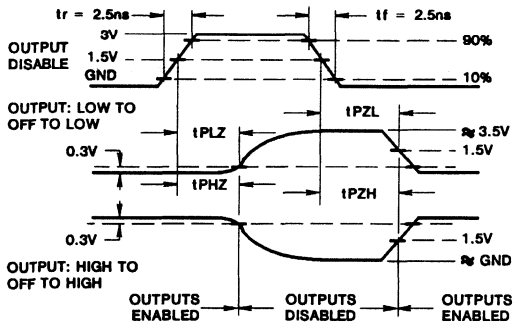
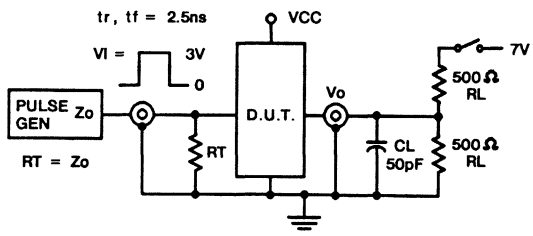


Figure 3 - Setup and hold times.

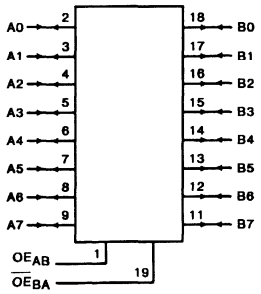




TEST	SWITCH POSITION
tPLZ, tPZL, OPEN DRAIN	CLOSED
tPHZ, tPZH, tPLH, tPHL	OPEN

Figure 4 - Three-state propagation delay times and test circuit.

CD54/74FCT7623



FUNCTIONAL DIAGRAM

Octal Bus Transceiver, 3-State (B Side), Open-Drain (A Side), Non-Inverting

Type Features:

- *Buffered inputs*
- *Typical Propagation delay: 5.2ns @ V_{CC} = 5V, T_A = +25°C, C_L = 50pF*

The CD54/74TCT7623 octal bus transceiver uses a small-geometry BiMOS technology. The output stages are a combination of bipolar and CMOS transistors that limits the output-HIGH level to two diode drops below V_{CC}. This resultant lowering of output swing (0V to 3.7V) reduces power bus ringing (a source of EMI) and minimizes V_{CC} bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enchances switching speed and is capable of sinking 48 to 64 milliamperes.

The CD54/74FCT7623 is a non-inverting 3-state bidirectional transceiver-buffer intended for two-way transmission from "A" bus to "B" bus or "B" bus to "A" bus, depending on the logic levels of the Output Enable (OE_{AB}, $\overline{OE}_{BA}$) inputs.

This design is a modified version of the CD54/74FCT623. It differs in that the 3-state outputs are on the B side only; the A side outputs are open drain.

The CD54/74FCT7623 is supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over two temperature ranges: Commercial (0°C to 70°C) and Extended Industrial (-55°C to +125°C).

The CD54FCT7623 is also available in chip form (H suffix). This unpackaged device is operable over the -55°C to +125°C temperature range.

Family Features:

- *SCR-latchup-resistant CMOS process and circuit design*
- *Speed of bipolar FAST*/AS/S with significantly reduced power consumption*
- *64/48-mA output sink current (commercial/extended industrial)*
- *Output voltage swing limited to 3.7V @ V_{CC} = 5V*
- *Controlled output-edge rates*
- *Input/output isolation to V_{CC}*
- *BiMOS technology with low quiescent power*

* FAST is a registered trademark of Fairchild Semiconductor Corp.

TRUTH TABLE

OUTPUT ENABLE INPUTS		OPERATION
$\overline{OE}_{BA}$	OE_{AB}	
L	L	B Data to (Open Drain) A Bus
H	H	A Data (TTL) to (3-State) B Bus
H	L	Isolation
L	H	B Data to (Open Drain) A Bus, A Data (TTL) to (3-State) B Bus

H = HIGH level
L = LOW level
To prevent excess currents in the HIGH-Z (isolation) modes, all I/O terminals should be terminated with 10kΩ to 1MΩ resistors.

Printed in USA/8-89

File Number **2358**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

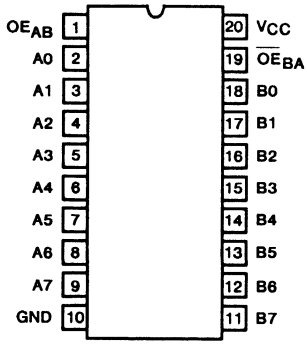
DC SUPPLY-VOLTAGE (V_{CC}) ..... -0.5V to 6V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5V$) ..... -20mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5V$) ..... -50mA
DC OUTPUT SINK CURRENT per Output Pin, I_O ..... +70mA
DC OUTPUT SOURCE CURRENT per Output Pin, I_O ..... -30mA
DC V_{CC} CURRENT (I_{CC}) 140mA
DC GROUND CURRENT (I_{GND}) 528mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55°C to +100°C (PACKAGE TYPE E) 500mW
For T_A = +100°C to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8mW/°C to 300mW
For T_A = -55°C to +70°C (PACKAGE TYPE M) 400mW
For T_A = +70°C to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6mW/°C to 70mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE E, M ..... -55°C to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 in. ± 1/32 in. (1.59mm ± 0.79mm) from case for 10s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59mm) with solder contacting lead tips only ..... +300°C

RECOMMENDED OPERATING CONDITIONS:

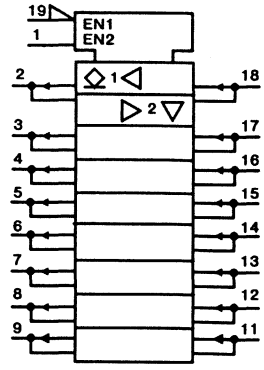
The following are normal operating ranges for these devices. For maximum reliability, devices should always be operated within these ranges.

CHARACTERISTIC		LIMITS MIN	LIMITS MAX	UNITS
Supply-Voltage Range, V_{CC}*:	CD74 Series, T_A = 0°C to 70°C	4.75	5.25	V
	CD54 Series, T_A = -55°C to +125°C	4.5	5.5	V
DC Input Voltage, V_I		0	V_{CC}	V
DC Output Voltage, V_O		0	$\leq V_{CC}$	V
Operating Temperature, T_A		-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv		0	10	ns/V

* Unless otherwise specified, all voltages are referenced to ground.



TERMINAL ASSIGNMENT



IEC LOGIC SYMBOL

STATIC ELECTRICAL CHARACTERISTICS

FCT Series: 74FCT Commercial Temperature Range, 0°C to +70°C; V_{CC} max = 5.25V, V_{CC} min = 4.75V
54FCT Extended Industrial Temperature Range, -55°C to +125°C; V_{CC} max = 5.5V, V_{CC} min = 4.5V

CHARACTERISTICS		TEST CONDITIONS			AMBIENT TEMPERATURE (T_A)						UNITS
					+25°C		0°C to +70°C		-55°C to +125°C		
		V_I (V)	I_O (mA)	V_{CC} (V)	MIN	MAX	MIN	MAX	MIN	MAX	
High-Level Input Voltage	V_{IH}			4.5 to 5.5	2	-	2	-	2	-	V
Low-Level Input Voltage	V_{IL}			4.5 to 5.5	-	0.8	-	0.8	-	0.8	V
High-Level Output Voltage	V_{OH}	V_{IH} or	-15	MIN	2.4	-	2.4	-	-	-	V
		V_{IL}	-12	MIN	2.4	-	-	-	2.4	-	V
Low-Level Output Voltage	V_{OL}	V_{IH} or	64	MIN	-	0.55	-	0.55	-	-	V
		V_{IL}	48	MIN	-	0.55	-	-	-	0.55	V
High-Level Input Current	I_{IH}	V_{CC}		MAX	-	0.1	-	1	-	1	µA
Low-Level Input Current	I_{IL}	GND		MAX	-	-0.1	-	-1	-	-1	µA
3-State Leakage Current	I_{OZH}	V_{CC}		MAX	-	0.5	-	10	-	10	µA
	I_{OZL}	GND		MAX	-	-0.5	-	-10	-	-10	µA
Short-Circuit Output Current *	I_{OS}	V_{CC} or GND $V_O = 0$		MAX	-60	-	-60	-	-60	-	mA
Input Clamp Voltage	V_{IK}	V_{CC} or GND	-18	MIN	-	-1.2	-	-1.2	-	-1.2	V
Quiescent Supply Current, MSI	I_{CC}	V_{CC} or GND	0	MAX	-	8	-	80	-	500	µA
Additional Quiescent Supply Current per Input Pin TTL Inputs High, 1 Unit Load	ΔI_{CC}	3.4V†		MAX	-	1.6	-	1.6	-	2	mA

* Not more than one output should be shorted at one time. Test duration should not exceed 100ms.
† Inputs that are not measured are at V_{CC} or GND.

FCT Input Loading: All inputs are 1 unit load. Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 1.6mA max. @ +70°C.

SWITCHING CHARACTERISTICS

FCT Series: t_r, t_f = 2.5ns, C_L = 50pF, R_L - See Figure 4

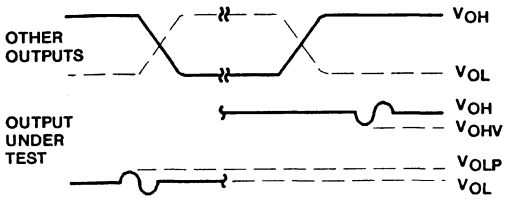
CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) 0°C to +70°C MIN	0°C to +70°C MAX	-55°C to +125°C MIN	-55°C to +125°C MAX	UNITS
Propagation Delays: A Data to B Bus	t_{PLH}, t_{PHL}	5†	1.5	7	1.5	7.5	ns
B Data to A Bus	t_{PZL}	5	1.5	7	1.5	7.5	ns
	t_{PLZ}	5	1.5	13	1.5	13.5	ns
Output Enable or Disable to Output 3-State (B Side)	t_{PZH}, t_{PZL} t_{PLZ}, t_{PHZ}	5	1.5	7.5	1.5	10	ns
Off-State Enabling, Disabling Times (A Side)	t_{PZL}, t_{PLZ}	5	1.5	9.5	1.5	10	ns
Power Dissipation Capacitance	C_{PD}§	-					pF
Min. (Valley) V_{OHV} (B Side) During Switching of Other Outputs (Output Under Test Not Switching)	V_{OHV} See Figure 1	5	0.5 Typical @ +25°C				V
Max. (Peak) V_{OLP} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OLP} See Figure 1	5	1 Typical @ +25°C				V
Input Capacitance	C_I	-	-	10	-	10	pF
3-State Output Capacitance (B Side)	C_O	-	-	15	-	15	pF
Off-State Output Capacitance (A Side)	C_O	-	-	15	-	15	pF

†5V: min. is @ 5.5V
max. is @ 4.5V
5V: min. is @ 5.25V for 0°C to +70°C
max. is @ 4.75V for 0°C to +70°C

§C_{PD}, measured per function, is used to determine the dynamic power consumption.
P_D (per package) = $V_{CC} I_{CC} + \Sigma (V_{CC}^2 f_i C_{PD} + V_O^2 f_o C_L + V_{CC} \Delta I_{CC} D)$ where:
V_{CC} = supply voltage
ΔI_{CC} = flow through current x unit load
C_L = output load capacitance
D = duty cycle of input high
f_o = output frequency
f_i = input frequency

3

PARAMETER MEASUREMENT INFORMATION



NOTES:

1. V_{OLP} is measured with respect to a ground reference near the output under test. V_{OHV} is measured with respect to V_{OH}.
2. Input pulses have the following characteristics: PRR ≤ 1MHz, t_r = 2.5ns, t_f = 2.5ns, skew 1ns.
3. R.F. fixture with 700-MHz design rules required. IC should be soldered into test board and bypassed with 0.1μF capacitor. Scope and probes require 700-MHz bandwidth.

Figure 1 - Simultaneous switching transient waveforms.

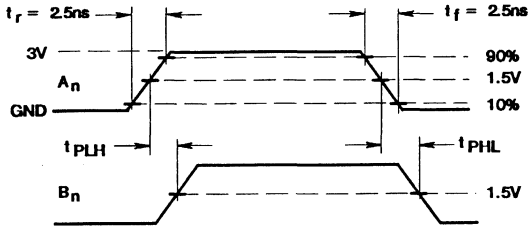


Figure 2 - Propagation delay times (A Data to B Bus).

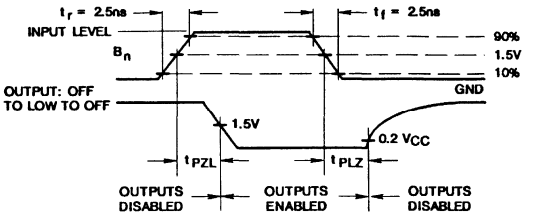
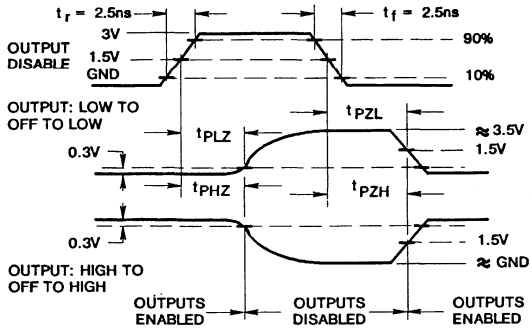
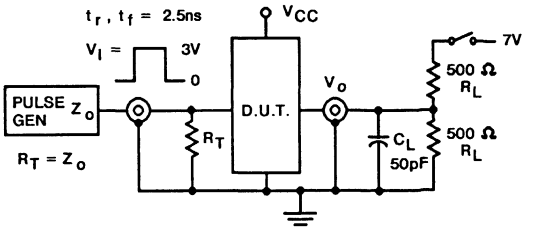


Figure 3 - Open-drain propagation delay times (B Data to A Outputs).

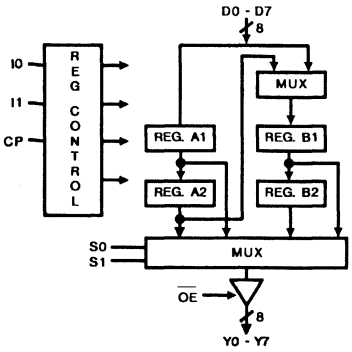




TEST	SWITCH POSITION
t_{PLZ}, t_{PZL}, OPEN DRAIN	CLOSED
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	OPEN

Figure 4 - Three-state propagation delay times and test circuit.

CD54/74FCT29520A, CD54/74FCT29521A



FUNCTIONAL DIAGRAM

Multilevel Pipeline Registers

Positive-Edge-Triggered

Type Features:

- *Buffered inputs*
- *Typical propagation delay: 3.5ns @ VCC = 5V, TA = 25°C, CL = 50pF*

3

The CD54/74FCT29520A and CD54/74FCT-29521A positive-edge-triggered multilevel pipeline registers use a small-geometry BiMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output-HIGH level to two diode drops below VCC. This resultant lowering of output swing (0V to 3.7V) reduces power bus ringing (a source of EMI) and minimizes VCC bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 32 to 48 milliamperes.

These devices each contain four 8-bit positive-edge-triggered registers that can be operated as a dual 2-level or as a single 4-level pipeline. A single 8-bit input, stored in any of the four registers, is available at the multiplexed 3-state output.

The CD54/74FCT29520A and CD54/74FCT29521A differ only in the way the data is loaded into and between the registers in the 2-level operation. (They operate identically in the single 4-level mode.) When data is entered into the first level of the CD54/74FCT29520A, the data stored in that level is moved into the second level. In the CD54/74FCT29521A, the same instructions (I0 = 0, I1 = 1 for A registers; I0 = 1, I1 = 0 for the B registers) simply cause the data in the first level to be overwritten. The transfer of data to the second level is accomplished by the instruction I0 = 0, I1 = 0. The transfer also causes the first level to change. In either device, I0 = 1, I1 = 1 initiates the HOLD mode. See Figure 1 for instructions/loading relationships.

The CD54/74FCT29520A and CD54/74FCT29521A are supplied in 24-lead dual-in-line narrow-body plastic packages (EN suffix) and in 24-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over two temperature ranges: Commercial (0°C to +70°C) and Extended Industrial (-55°C to +125°C).

Family Features:

- *SCR-latchup-resistant CMOS process and circuit design*
- *Speed of bipolar FAST*/AS/S with significantly reduced power consumption*
- *48/32-mA output sink current (commercial/extended industrial)*
- *Output voltage swing limited to 3.7V @ VCC = 5V*
- *Controlled output-edge rates*
- *Input/output isolation to VCC*
- *BiMOS technology with low quiescent power*

* FAST is a registered trademark of Fairchild Semiconductor Corp.

The CD54FCT29520A and CD54FCT29521A are also available in chip form (H suffix). These unpackaged devices are operable over the -55°C to +125°C temperature range.

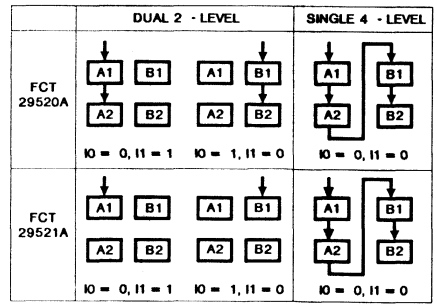


Figure 1 - Data loading vs. instructions.

Printed in USA/8-89

File Number **2401**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (VCC) ..... -0.5V to 6V
DC INPUT DIODE CURRENT, IIK (for VI < -0.5V) ..... -20mA
DC OUTPUT DIODE CURRENT, IOK (for VO < -0.5V) ..... -50mA
DC OUTPUT SINK CURRENT per Output Pin, IO ..... +70mA
DC OUTPUT SOURCE CURRENT per Output Pin, IO ..... -30mA
DC VCC CURRENT (ICC) 260mA
DC GROUND CURRENT (IGND) 400mA
POWER DISSIPATION PER PACKAGE (PD):
For TA = -55°C to +100°C (PACKAGE TYPE E) 500mW
For TA = +100°C to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8mW/°C to 300mW
For TA = -55°C to +70°C (PACKAGE TYPE M) 400mW
For TA = +70°C to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6mW/°C to 70mW
OPERATING-TEMPERATURE RANGE (TA):
PACKAGE TYPE E, M ..... -55°C to +125°C
STORAGE TEMPERATURE (Tstg) ..... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 in. ± 1/32 in. (1.59mm ± 0.79mm) from case for 10s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59mm) with solder contacting lead tips only ..... +300°C

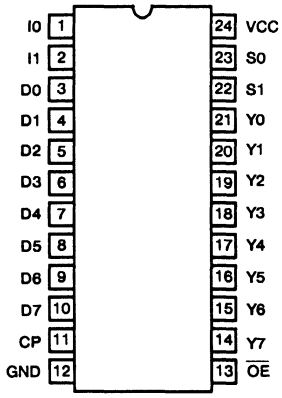
RECOMMENDED OPERATING CONDITIONS:

The following are normal operating ranges for these devices. For maximum reliability, devices should always be operated within these ranges.

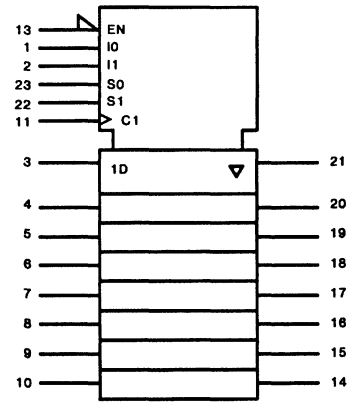
CHARACTERISTIC		LIMITS MIN	LIMITS MAX	UNITS
Supply-Voltage Range, VCC*:	CD74 Series, TA = 0°C to 70°C	4.75	5.25	V
	CD54 Series, TA = -55°C to +125°C	4.5	5.5	V
DC Input Voltage, VI		0	VCC	V
DC Output Voltage, VO		0	≤ VCC	V
Operating Temperature, TA		-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv		0	10	ns/V

* Unless otherwise specified, all voltages are referenced to ground.

CD54/74FCT29520A AND CD54/74FCT29521A



TERMINAL ASSIGNMENT



IEC LOGIC SYMBOL

STATIC ELECTRICAL CHARACTERISTICS

FCT Series: 74FCT Commercial Temperature Range, 0°C to +70°C; VCC max = 5.25V, VCC min = 4.75V
54FCT Extended Industrial Temperature Range, -55°C to +125°C; VCC max = 5.5V, VCC min = 4.5V

CHARACTERISTICS		TEST CONDITIONS VI (V)	TEST CONDITIONS IO (mA)	VCC (V)	AMBIENT TEMPERATURE (TA) +25°C MIN	+25°C MAX	0°C to +70°C MIN	0°C to +70°C MAX	-55°C to +125°C MIN	-55°C to +125°C MAX	UNITS
High-Level Input Voltage	VIH			4.5 to 5.5	2	-	2	-	2	-	V
Low-Level Input Voltage	VIL			4.5 to 5.5	-	0.8	-	0.8	-	0.8	V
High-Level Output Voltage	VOH	VIH or	-24	MIN	2.4	-	2.4	-	-	-	V
		VIL	-20	MIN	2.4	-	-	-	2.4	-	V
Low-Level Output Voltage	VOL	VIH or	48	MIN	-	0.55	-	0.55	-	-	V
		VIL	32	MIN	-	0.55	-	-	-	0.55	V
High-Level Input Current	IIH	VCC		MAX	-	0.1	-	1	-	1	µA
Low-Level Input Current	IIL	GND		MAX	-	-0.1	-	-1	-	-1	µA
3-State Leakage Current	IOZH	VCC		MAX	-	0.5	-	10	-	10	µA
	IOZL	GND		MAX	-	-0.5	-	-10	-	-10	µA
Short-Circuit Output Current *	IOS	VCC or GND VO = 0		MAX	-60	-	-60	-	-60	-	mA
Input Clamp Voltage	VIK	VCC or GND	-18	MIN	-	-1.2	-	-1.2	-	-1.2	V
Quiescent Supply Current, MSI	ICC	VCC or GND	0	MAX	-	8	-	80	-	500	µA
Additional Quiescent Supply Current per Input Pin TTL Inputs High, 1 Unit Load	ΔICC	3.4V†		MAX	-	1.6	-	1.6	-	2	mA

* Not more than one output should be shorted at one time. Test duration should not exceed 100ms.
† Inputs that are not measured are at VCC or GND.

FCT Input Loading: All inputs are 1 unit load. Unit load is ΔICC limit specified in Static Characteristics Chart, e.g., 1.6mA max. @ +70°C.

PREREQUISITE FOR SWITCHING

CHARACTERISTICS	SYMBOL	VCC (V)	AMBIENT TEMPERATURE (TA) 0°C to +70°C MIN	0°C to +70°C MAX	-55°C to +125°C MIN	-55°C to +125°C MAX	UNITS
Clock Pulse Width	tW	5†	7	-	8	-	ns
Setup Time — Data to Clock, Instruction to Clock	tSU	5	5	-	6	-	ns
Hold Time — Data to Clock, Instruction to Clock	tH	5	1	-	2	-	ns
Maximum Clock Frequency	fMAX	5	70	-	60	-	MHz

†5V: min. is @ 4.5V
5V: min. is @ 4.75V for 0°C to +70°C

SWITCHING CHARACTERISTICS

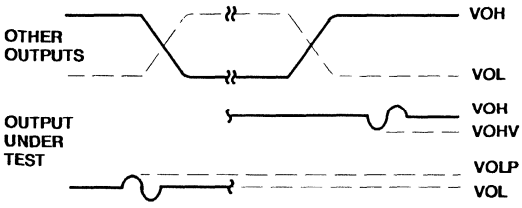
FCT Series: tr, tf = 2.5ns, CL = 50pF, RL - See Figure 5

CHARACTERISTICS	SYMBOL	VCC (V)	AMBIENT TEMPERATURE (TA) 0°C to +70°C MIN	0°C to +70°C MAX	-55°C to +125°C MIN	-55°C to +125°C MAX	UNITS
Propagation Delays: Clock to Output	tPLH, tPHL	5†	1.5	14	1.5	16	ns
Select to Output	tPLH, tPHL	5	1.5	13	1.5	15	ns
Output Disable to Output	tPLZ, tPHZ	5	1.5	15	1.5	16	ns
Output Enable to Output	tPZL, tPZH	5	1.5	12	1.5	13	ns
Power Dissipation Capacitance	CPD§	-					pF
Min. (Valley) VOHV During Switching of Other Outputs (Output Under Test Not Switching)	VOHV See Figure 2	5	0.5 Typical @ +25°C				V
Max. (Peak) VOLP During Switching of Other Outputs (Output Under Test Not Switching)	VOLP See Figure 2	5	1 Typical @ +25°C				V
Input Capacitance	CI	-	-	10	-	10	pF
3-State Output Capacitance	CO	-	-	15	-	15	pF

†5V: min. is @ 5.5V
max. is @ 4.5V
5V: min. is @ 5.25V for 0°C to +70°C
max. is @ 4.75V for 0°C to +70°C

§CPD, measured per flip-flop, is used to determine the dynamic power consumption.
PD (per package) = VCC ICC + Σ (VCC^2 fi CPD + VO^2 fo CL + VCC ΔICC D) where:
VCC = supply voltage
ΔICC = flow through current x unit load
CL = output load capacitance
D = duty cycle of input high
fo = output frequency
fi = input frequency

PARAMETER MEASUREMENT INFORMATION



NOTES:

1. VOLP is measured with respect to a ground reference near the output under test. VOHV is measured with respect to VOH.
2. Input pulses have the following characteristics: PRR ≤ 1MHz, tr = 2.5ns, tf = 2.5ns, skew 1ns.
3. R.F. fixture with 700-MHz design rules required. IC should be soldered into test board and bypassed with 0.1μF capacitor. Scope and probes require 700-MHz bandwidth.

Figure 2 - Simultaneous switching transient waveforms.

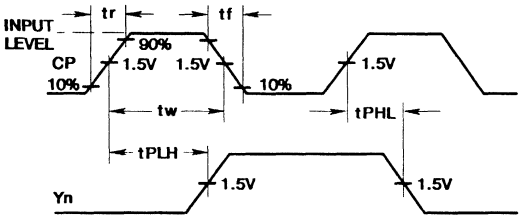


Figure 3 - Propagation delay times.

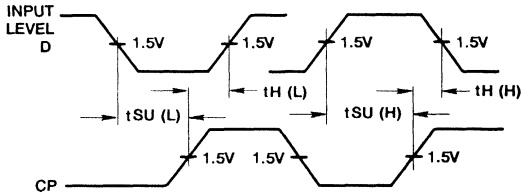
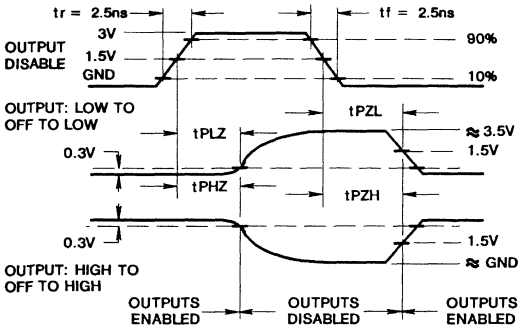
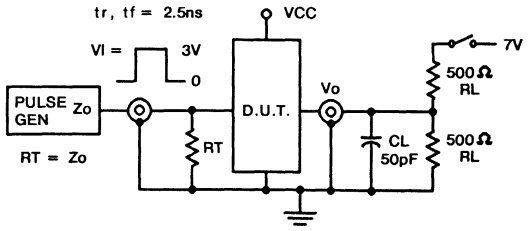


Figure 4 - Setup and hold times.





TEST	SWITCH POSITION
tPLZ, tPZL, OPEN DRAIN	CLOSED
tPHZ, tPZH, tPLH, tPHL	OPEN

Figure 5 - Three-state propagation delay times and test circuit.

Application Note

4

Application Note

FCT CMOS Logic Optimized for Backplane Interface

By W. Austin and B. Petryna

We are now at a new threshold in CMOS design capability, adding enhancement features and modifying the basic technology to support bipolar adaptations. Our purpose in this Note is to look at bus drive requirements and the advantages to be gained by applying these new techniques to a modified CMOS structure. A newly developed Harris FCT logic design is primarily a CMOS structure having the advantages needed to drive a VME-bus backplane.

Much has been said about the advantages of Advanced High-Speed CMOS Logic, devices as bus drivers for a VME bus or equivalent bus system. The basic advantages of CMOS in any high-performance system application are well known. The speed capability developed in the new families of AC/ACT and FCT is now second only to that of the ECL and GaS technologies. The classic qualities of CMOS low-power consumption and excellent noise immunity cannot be overstated. The wide operating-temperature range of CMOS with minimal change in electrical characteristics is important to the performance and reliability of any system. These merits have been demonstrated in HC/HCT versus LSTTL logic and AC/ACT versus FAST* logic. These qualities are retained in the latest Harris FCT logic circuits.

VME-Bus Conditions

While the specifications for a VME bus, such as the one illustrated in Fig. 1, are defined for bipolar integrated circuits, no restrictions are placed on the use of any technology that can produce equal or better results. The application techniques for AC/ACT logic driving the VME bus or an equivalent data bus system have been explored. AC/ACT logic does have considerable application potential, but also has limited drive capability. AC/ACT logic is defined for 24-mA sink and source drive, while the VME-bus specifications call for 48 and 64-mA sink current to drive several of the backplane lines. The VME bus may have as many as 21 slots spaced over 500 mm (19.7 inches), with 2 pF (no load) to 20 pF per slot. The combined capacitance loading and low characteristic impedance of each bus "stripline" gives rise to the need for high current drive to support the high-speed data rates of the bus.

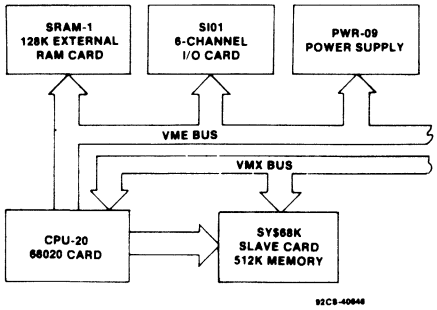


Fig. 1 - VME-bus system block diagram.

The bus tolerance specifications for power-supply voltage are relatively tight, giving rise to another bus design problem. It must be recognized that imbalance in power supplies does exist. Imbalance may occur with deteriorating conditions of contact resistance or separate system power-supply changes and any irregular conditions that produce transients on the line. The imbalance, if sufficient, can overdrive protection and substrate diodes at the input and output of CMOS devices. While the problem can be resolved by various design techniques, "bus hang-up" resulting from power-supply imbalance can be resolved more directly by the use of Harris FCT logic circuits. On-chip circuit design features include current-blocking diode junctions to prevent differential-power-supply imbalance problems.

A VME-Bus Model

The VME-bus lines may be characterized by a given set of modeling information. As shown in Fig. 2(a), if we use a microstrip circuit element 0.1 inch in length, each PC board microstrip element of line has 0.129 pF of shunt capacitance and 1.561 nH of series inductance, for which the line characteristic impedance (Z_O) is:

$$Z_O = (L/C) \text{ exp } 0.5$$
$$= (1.561 \text{ nH}/0.129 \text{ pF}) \text{ exp } 0.5$$
$$= 110 \text{ ohms}$$

And, as a model to determine drive requirements, a slot-to-slot segment consists of eight sections of the 0.1-inch element. If we include the 2 pF per empty slot on the VME-bus line as a distributed capacitance, the Z_O becomes 64 ohms. VME-bus rules state that the characteristic impedance for each unloaded "microstrip-line" is recommended to be approximately 100 ohms, not including slot capacitance loading. The backplane as a line may be configured by choice as end driven or center driven, although some slot positions, such as the system clock driver (specified to slot no. 1) are predetermined. Various configurations are shown in Figs. 2(b) and 2(c). For the purposes of modeling, the slot load is identified as an occupied slot with the characteristics shown in Fig. 2(d).

*FAST is a Registered Trademark of Fairchild Semiconductor Corp.

Printed in USA/10-88

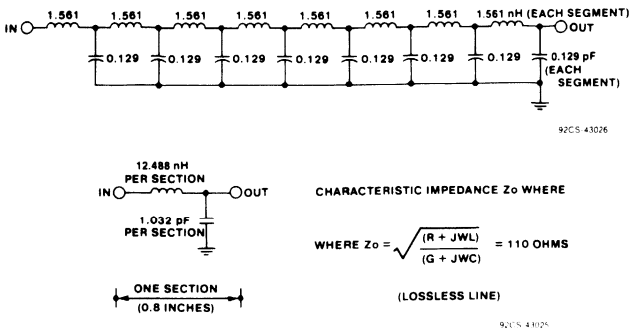


Fig. 2(a) - Cascade of 0.1-inch microstrip-line elements used to simulate each 0.8-inch of a slot-to-slot line segment.

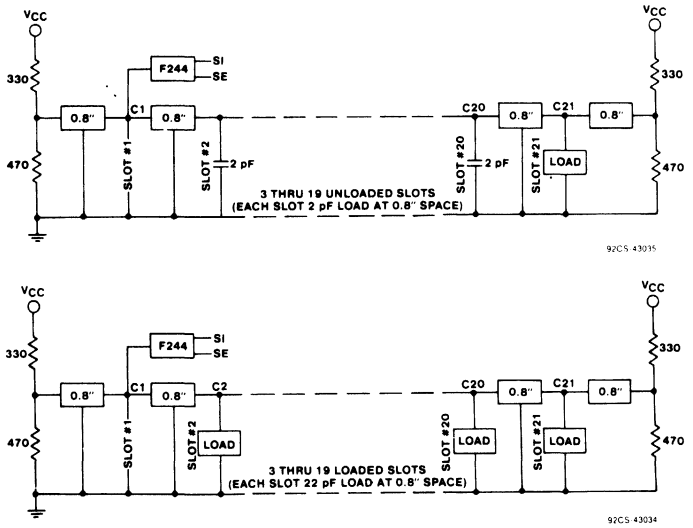


Fig. 2(b) - Test-circuit simulation model for an end-driven VME-bus line: unloaded (top) and loaded (bottom).

While the configuration described in Fig. 2 was established for modeling, it is our intent here to note the performance of the Harris FCT versus AC/ACT and FAST line drivers in this representative system. Using a defined number of slots as loads on the VME bus, the performance characteristics of the Harris FCT line drivers in a VME-bus application are shown.

The line terminations are defined for both ends of the VME bus as 330 and 470 ohms in series or a Thevenin equivalent of 2.94 volts and 194 ohms. It is readily apparent that the resistive load is a major concern for power requirements on the bus. FCT and CMOS bus drivers may be designed to have only a few ohms of channel resistance to meet the bus drive-level requirements and, by the defined standard, imitate the bipolar characteristics as a bus driver. The standard VME-bus termination is shown in the circuit of Fig. 3.

As noted, when capacitance is added at the distributed slots in the backplane, we are effectively changing the Z_O of the line. With more distributed line capacitance, the Z_O of the line is lower, making the line termination a greater (higher) mismatch in impedance. This increased mismatch, and irregular loading, will cause more line reflections. It is a primary concern here to show that the reflections, as well as ringing and other noise on the line, does not exceed a specified level of noise immunity while still meeting the timing requirements of the line. The device selected to demonstrate the VME-bus drive capability is the FCT 240. The structure we have chosen for demonstration is a standard VME backplane with nine slots filled. A block diagram of the test fixture is shown in Fig. 4.

Differential Power-Supply Problems

Power-supply imbalance on the VME bus may cause the bus to hang up when drivers operate from unequal power-

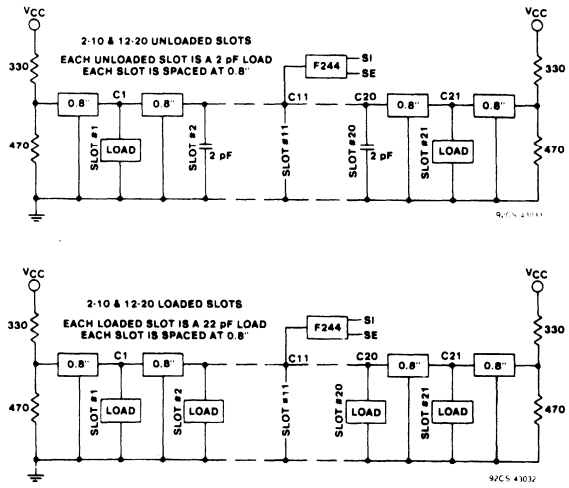


Fig. 2(c) - Test-circuit simulation model for a center-driven VME-bus line: unloaded (top) and loaded (bottom).

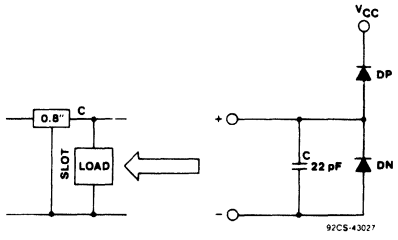


Fig. 2(d) - CMOS-equivalent slot load on the bus line.

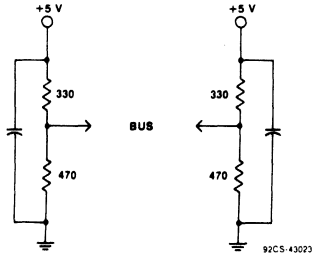


Fig. 3 - Standard VME-bus termination.

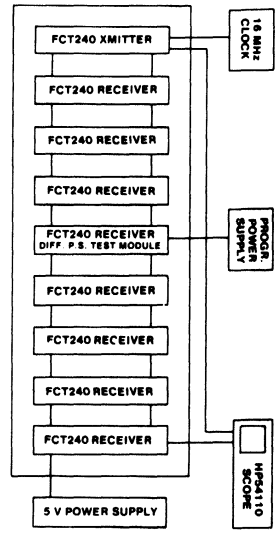


Fig. 4 - Block diagram of the VME-bus backplane test chassis.

supply levels across the length of the bus. For obvious reasons, the specifications for the power supplies must be very tight. The bus tolerance specification for the +5 volt supplies are +0.25/–0.125 volt. However, under stress conditions with added voltage drop in the contacts and lines, it is probable that some switching conditions will cause the line voltage to exceed the standard power-supply tolerance and the nominal IC specification of V_{CC} + 0.5 volts. Nearly all computer systems have board-to-board or frame-to-frame power-supply differences, which can cause bus-driver problems. There are various ways to accommodate this imbalance, such as the use of diodes to prevent excessive current when on-chip diode junctions are reversed. Where AC/ACT or HC/HCT CMOS is used, the common technique illustrated in Fig. 5 may be used to prevent reverse current through the IC.

While line drivers may be designed with CMOS technology to meet all specified signal switching levels for the VME bus, and avoid power supply problems by using the blocking diodes of Fig. 5, the technique may be regarded as a problem fix and not a design solution. All line receivers or operational transceiver devices require the protection because of the potential problem at the receiving end of the line. Drawbacks are noted with the use of diodes, such as the need for low forward-voltage drop equivalent to the Schottky barrier diodes. The diode adds to the power-supply tolerance problems and reduces the noise immunity of the system. Still, this does not change the fact that standard CMOS designs have input and output diodes that will reverse when overdriven. And, without protection, the condition of overdrive on the bus can cause hangups and timing-delay problems, as well as overdissipation.

The design of Harris FCT output driver structures includes protection to prevent driver interfaced loading on the bus during wide ranging of power-supply differential voltage. Given a separate supply for an FCT-loaded line driver, variations of zero to maximum V_{DD} will not cause the backplane line to be loaded. Measurement results verify the design goals as noted above.

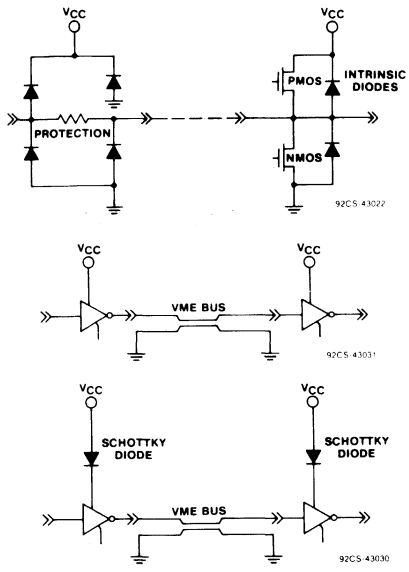


Fig. 5 - AC/ACT driver interface to the VME bus with Schottky-diode recommendation to solve differential power-supply problem.

Harris FCT Circuit Description

The requirements for backplane interface applications are similar to those associated with a bipolar transistor circuit (i.e., speed, high drive current, and limited voltage swings). Although small geometry CMOS devices can meet the performance criteria of bipolar devices, the inherent rail-to-rail output-voltage swing of CMOS devices generates greater switching noise and reflected energy in a bus environment. The electrical requirements for the Harris FCT output buffer circuit are:

1. High output sink current (I_{OL} = 64 mA for commercial/military grade) so that the output voltage swing is monotonic to the input threshold voltage (V_{IL} max.).
2. Reduced voltage swings and controlled output edge rates to minimize noise generation and reflected energy.
3. Output/Input isolation to V_{CC} to eliminate differential power-supply problems where devices may be powered through input/output structures.
4. Low quiescent power dissipation similar to that of a pure CMOS device.

These requirements are satisfied by the Harris FCT output buffer design illustrated in Fig. 6. The description of the output circuit can be divided into two parts, the pull-up and the pull-down circuit. The pull-up circuit consists of two active elements, an NMOS and n-p-n transistor. The NMOS transistor is the switching element that pulls the output from the V_{OL} through the output switch point (1.5V). The n-p-n transistor is the output-voltage-level element that limits the V_{OH} level to 2 V_{BE} below the supply voltage. This pull-up circuit configuration isolates V_{CC} from the output. The pull-down circuit consists of a distributed NMOS, which is turned on sequentially to control the switching current transients and the output skew rate (dv/dt). This control is combined with a limited voltage swing to minimize switching noise and reflected energy on the backplane.

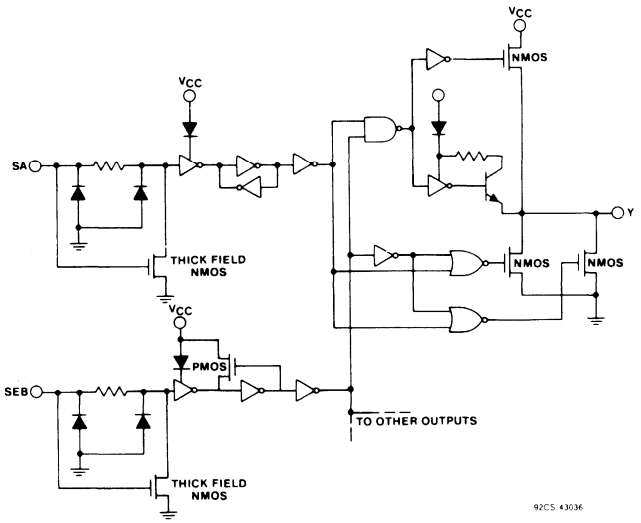


Fig. 6 - Logic diagram of the Harris FCT driver circuit.

Measured Drive Data

To establish measured capability for the simulated FCT VME bus driver, the simulation curves of Fig. 7(a) were run with alternate slots loaded to show significant points of comparison in typical curves. Theoretical results show that the end of the line drives to a higher level than the input if the matching impedance is higher than the characteristic impedance. This is the case in Fig. 7(a) where slot 21 shows

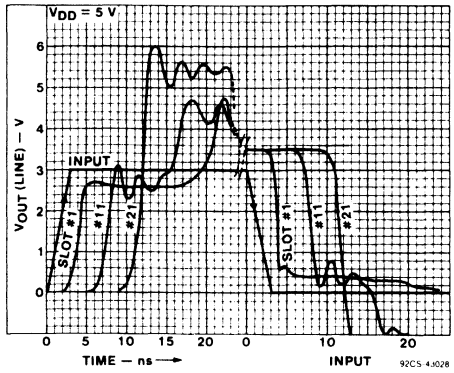


Fig. 7(a) - VME-bus simulated curves for typical conditions with loading in the odd-numbered slots.

levels rising to an overshoot of more than 5 volts with some ringing. It is for this reason that FCT switching levels are typically 3 volts. Similar results occur in the negative step as the output goes below the ground level, but is otherwise clamped by the load diodes. Fig. 7(b) is added to show a fully loaded VME bus; waveforms are shown for slots 1, 11, and 21. This is a worst-case condition for the same simulation parameters used to drive the bus. Due to the added loading, the overshoots are less, but the settling time is longer. It should be noted that a fully loaded bus is not common design practice because of close spacing and mechanical size limitations.

Another significant point of comparison is the initial and final settling levels of the input step for both directions of

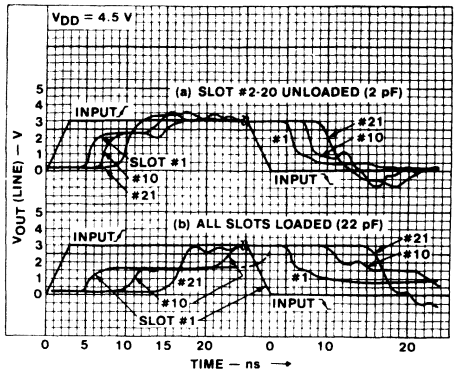


Fig. 7(b) - Worst-case VME-bus simulation plots: unloaded (top) and all slots loaded (bottom).

switching. On the rising edge of the pulse, an initial setup level of change occurs before finally settling to the high pull-up level. This transitional change is less as we move further down the bus line. When the change is in the negative direction, similar undershoot or overshoot occurs, depending on the position on the line. Sufficient drive requirement is needed at line drive input to pull the negative transition firmly to ground without a ringing bounce on the line. The initial step change must stay below the specified V_{IL} level for TTL, a condition that may be difficult to meet if the driver is not designed for 64 mA of sink current.

Measured comparisons of FCT240, F240, ACT240, and IDT240 drivers are shown in Figs. 8 through 11, where 8(a), 9(a), 10(a), and 11(a) show loaded (see Fig. 4) and 8(b), 9(b), 10(b), and 11(b) unloaded conditions. In this set of measurements, the VME bus chosen for test had resistive-load terminations in slots 1 and 21, a driver in slot 2, a receiver in slot 20, and loads in the even slots, but no plug-in module at slot 16.

The FCT240 data is similar to that of the simulated condition, but with less ringing and at a lower frequency. The rise-time edge rates for all waveforms are much less than the normal delay time for the VME bus as shown, which is about 8 ns loaded and 5 ns unloaded. The rising edge exceeds the 5V supply level to about twice the input drive level; similar conditions on the falling edge show a negative transition to about -1 volt. Protection diodes at the input provide clamping, which dampens any negative swing.

The F240 curves of Figs 9(a) and 9(b) show similar results except for more damped conditions due to the input loading characteristic of the bipolar devices. The rise time is somewhat slower than the FCT and the propagation delay is noted to be essentially the same as for the FCT. In general, the F240 and FCT240 have similar characteristics except for the faster rise time and the peak voltage swing for the FCT device.

The performance of the ACT device is shown in Fig. 10 for comparison. The performance of the ACT240 is similar to the F240 and FCT240 for the VME-bus test fixture used. Under the loaded conditions shown, the trailing edge is slower to settle to zero. The rising edge pull-up is much stronger, which for most switching applications is an advantage. As a driver for the VME bus, under loaded or loaded-line conditions, the ACT output reaches a level of 7.5 volts. This value is marginally over the maximum V_{DD} ratings. The use of a dropping diode in the V_{DD} line should serve as a means to keep the maximum positive level within ratings, as well as to resolve any differential-power-supply system problems.

Bibliography

1. "Using Advanced CMOS Logic in a VME Data Bus System," J. Nadolski and A. Kalish, GE Solid State Application Note ICAN-8640.
2. Motorola VME-Bus Specification Manual, MICROSYSTEMS MVMEBS/D2, Revision C.
3. "Powering VME-Bus Systems," W. Yates, Electronics Products, Jan. 15, 1988.

Acknowledgments

Measurement data taken by E. Wittmann; circuit modeling and simulation data done by C. Hsu.

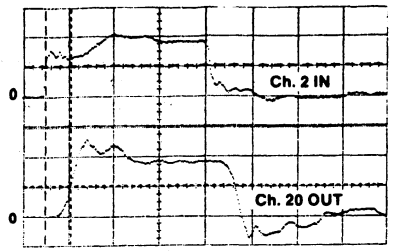


Fig. 8(a) - RCA FCT240 loaded.

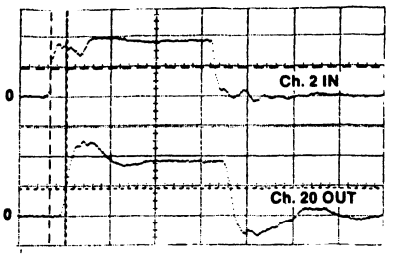


Fig. 8(b) - RCA FCT240 unloaded.

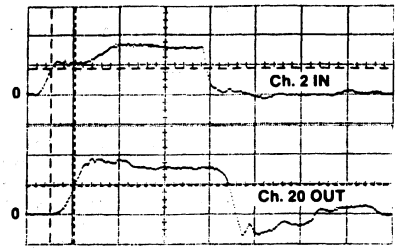


Fig. 9(a) - F240 loaded.

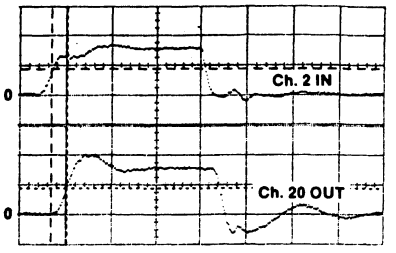


Fig. 9(b) - F240 unloaded.

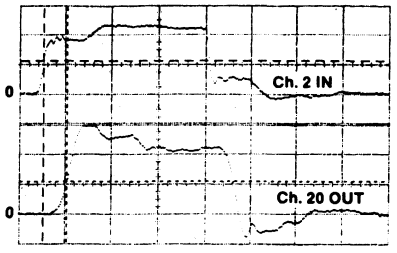


Fig. 10(a) - RCA ACT240 loaded.

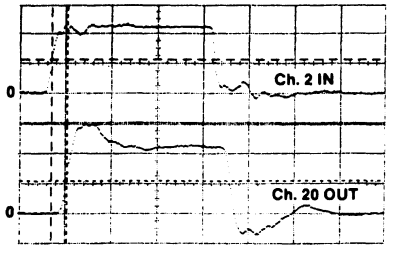


Fig. 10(b) - RCA ACT240 unloaded.

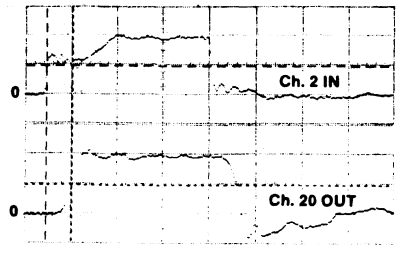


Fig. 11(a) - IDT 240 loaded.

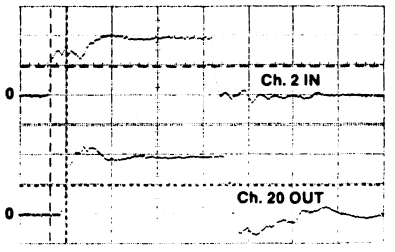


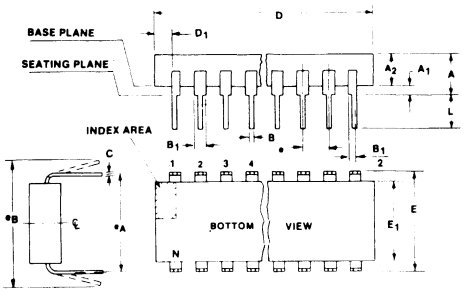
Fig. 11(b) - IDT 240 unloaded.

Figs. 8 to 11 - VME-bus measurements comparing line drivers (Fig. 4 test fixture):
Channel 1 (top) = 2.5 V/div (vertical)
Channel 2 (bottom) = 2.5 V/div (vertical)
Timebase = 15.0 ns/div (horizontal)
(a) Backplane with even slots loaded; driver slot 2 (top waveform); receiver slot 20 (bottom waveform)
(b) Backplane with slots 3 to 19 unloaded; driver slot 2 (top waveform); receiver slot 20 (bottom waveform).

Dimensional Outlines

5

Dual-In-Line Plastic Packages



Notes:

1. Refer to JEDEC Publication No. 95 JEDEC Registered and Standard Outlines for Solid State Products, for rules and general information concerning registered and standard outlines, in Section 2.2.
2. Protrusions (flash) on the base plane surface shall not exceed 0.010 in. (0.25 mm).
3. The dimension shown is for full leads. "Half" leads are optional at lead positions

   $1, N, \frac{N}{2}, \frac{N}{2}+1.$
4. Dimension D does not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 in. (0.25 mm).
5. E is the dimension to the outside of the leads and is measured with the leads perpendicular to the base plane (zero lead spread).
6. Dimension E_1 does not include mold flash or protrusions.
7. Package body and leads shall be symmetrical around center line shown in end view.
8. Lead spacing e shall be non-cumulative and shall be measured at the lead tip. This measurement shall be made before insertion into gauges, boards or sockets.
9. This is a basic installed dimension. Measurement shall be made with the device installed in the seating plane gauge (JEDEC Outline No. GS-3, seating plane gauge). Leads shall be in true position within 0.010 in. (0.25 mm) diameter for dimension e_A.
10. e_B is the dimension to the outside of the leads and is measured at the lead tips before the device is installed. Negative lead spread is not permitted.
11. N is the maximum number of lead positions.
12. Dimension D_1 at the left end of the package must equal dimension D_1 at the right end of the package within 0.030 in. (0.76 mm).
13. For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package centerlines.

(E) Suffix (JEDEC MS-001-AE)
20-Lead Dual-In-Line Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.210	—	5.33	9
A_1	0.015	—	0.39	—	9
A_2	0.115	0.195	2.93	4.95	
B	0.014	0.022	0.356	0.558	
B_1	0.045	0.070	1.15	1.77	3
C	0.008	0.015	0.204	0.381	
D	0.925	1.060	23.5	26.9	4
D_1	0.005	—	0.13	—	12
E	0.300	0.325	7.62	8.25	5
E_1	0.240	0.280	6.10	7.11	6, 7
e	0.100 BSC		2.54 BSC		8
e_A	0.300 BSC		7.62 BSC		9
e_B	—	0.430	—	10.92	10
L	0.115	0.160	2.93	4.06	9
N	20		20		11

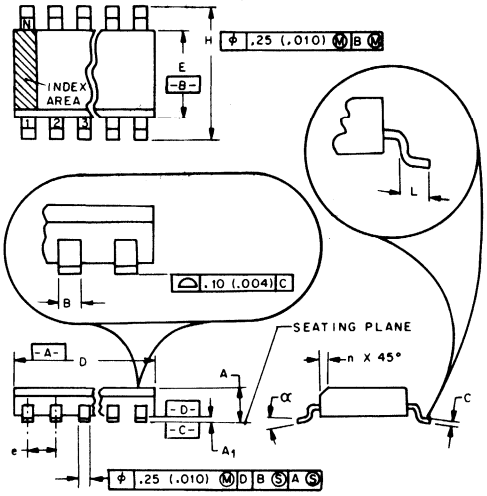
92CS-39997

(EN) Suffix (JEDEC MS-001-AF)
24-Lead Dual-In-Line Narrow-Body Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.210	—	5.33	9
A_1	0.015	—	0.39	—	9
A_2	0.115	0.195	2.93	4.95	
B	0.014	0.022	0.356	0.558	
B_1	0.045	0.070	1.15	1.77	3
C	0.008	0.015	0.204	0.381	
D	1.125	1.275	28.6	32.3	4
D_1	0.005	—	0.13	—	12
E	0.300	0.325	7.62	8.25	5
E_1	0.240	0.280	6.10	7.11	6, 7
e	0.100 BSC		2.54 BSC		8
e_A	0.300 BSC		7.62 BSC		9
e_B	—	0.430	—	10.92	10
L	0.115	0.160	2.93	4.06	9
N	24		24		11

92CS-39943

Dual-In-Line Small-Outline Plastic Packages



NOTES:

1. Refer to applicable symbol list.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. "D" is a reference datum.
4. "A" and "B" are reference datums and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm (0.006 in.).
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the cross-hatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Controlling dimensions: MILLIMETERS.

M Suffix (JEDEC MS-013AC)
20-Lead Dual-In-Line
Small-Outline (SO) Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.0926	0.1043	2.35	2.65	
A_1	0.0040	0.0118	0.10	0.30	
B	0.0138	0.020	0.35	0.508	
C	0.0091	0.0125	0.23	0.32	
D	0.4961	0.5118	12.60	13.00	4
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		
H	0.394	0.419	10.00	10.65	
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	20		20		7
α	0°	8°	0°	8°	

Notes: 1, 2, 3, 8, 9

92CS-38926R2

M Suffix (JEDEC MS-013AD)
24-Lead Dual-In-Line
Small-Outline (SO) Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.0926	0.1043	2.35	2.65	
A_1	0.0040	0.0118	0.10	0.30	
B	0.0138	0.020	0.35	0.508	
C	0.0091	0.0125	0.23	0.32	
D	0.5985	0.6141	15.20	15.60	4
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		
H	0.394	0.419	10.00	10.65	
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	24		24		7
α	0°	8°	0°	8°	

Notes: 1, 2, 3, 8, 9

92CS-39037R2

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